Vivado
New Project Tutorial

This tutorial guides you through the typical steps of design, simulation, synthesis and implementation of a simple project, designed from scratch, like those that you will do at the Applications for the Digital Integrated Circuits course.

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Project File Management

The FPGA design flow goes through the stages shown in Figure 1. The Vivado IDE (Integrated Design Environment) arranges these stages in the *Flow Navigator* and guides you through it.

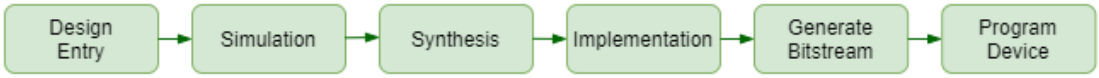


Figure 1: FPGA design flow

Various files are employed in each design flow stage, all of them created and managed by Vivado, except for the source files, that are written by you, the designer. All files created by Vivado reside in the project folder (directory) and its subfolders. Your source files should also reside inside the project folder.

To keep things as simple as possible, strictly follow these two rules:

- **Each project has its own folder.**
- **All (Verilog) source files are saved in their default locations.**

The project folder has the structure shown in Figure 2.

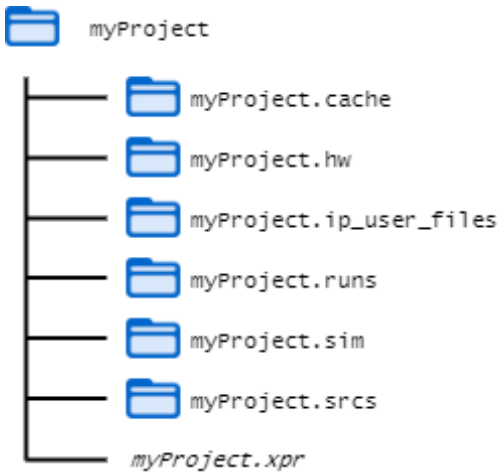


Figure 2: Vivado project folder structure.

Some folders are created by Vivado at the project creation, others are created during later stages of the FPGA design flow. Most of the files are taken care of by Vivado, so you need not bother about their names or where they are located. The only files you should care about are:

- design source files
- simulation source files
- constraints file

Remember:

- **All project source files should reside inside the project folder.**

Create a New Project

Open the Vivado program. Wait a couple seconds until Vivado opens the Start Page.

From the Start Page open the New Project wizard by clicking on **Create Project** option in the **Quick Start** panel (Figure 3). Alternatively you may open the New Project wizard from Vivado's main menu, selecting **File** -> **New Project …** .

Figure 3: Quick Start panel from Vivado Start Page

The New Project wizard opens a dialog with a brief description of the wizard (Figure 4). Click **Next** to advance through the New Project wizard steps.

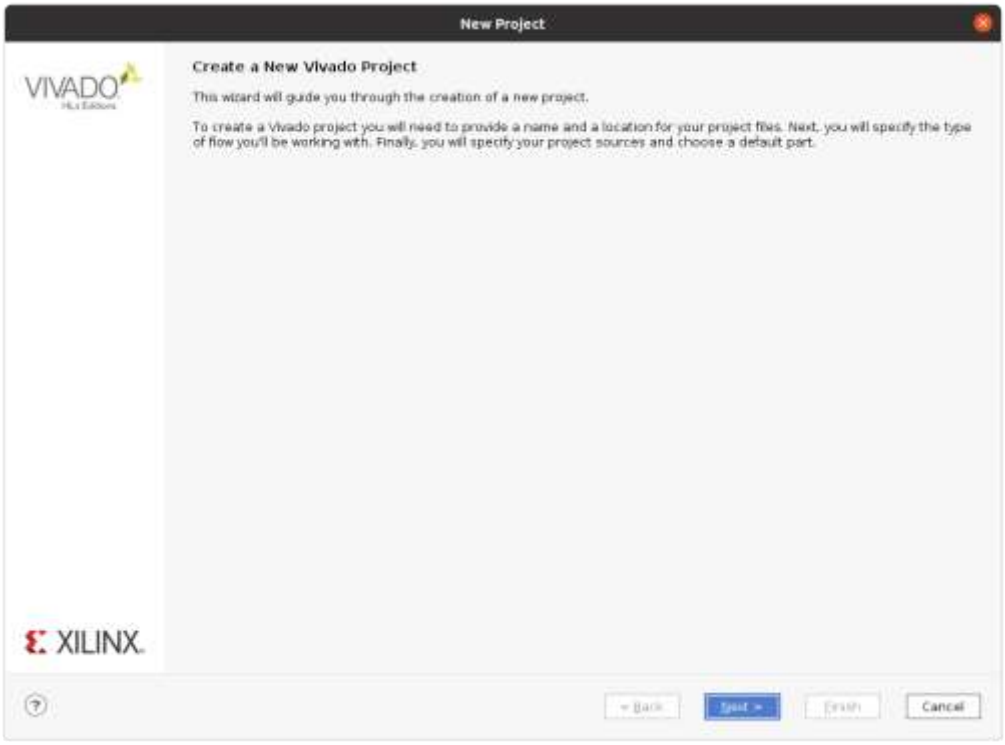


Figure 4: New Project wizard open dialog

In step 1 (Project Name) of the New Project wizard (Figure 5) set the name of the project in the *Project Name* text editor field. The default name is `project_1`, but you should change it to a more descriptive name. Vivado uses this name as a prefix for the names of the project's subfolders.

Check the checkbox *Create project subdirectory*. You may keep the default *Project Location* (`/home/student on Linux`) or change it to a convenient location but be sure to create a project subdirectory such that all project files are kept in its subdirectory and not mixed with other files, unrelated to this project. If a warning message appears, telling you that a subdirectory with this name already exists, you should change the *Project Name.*

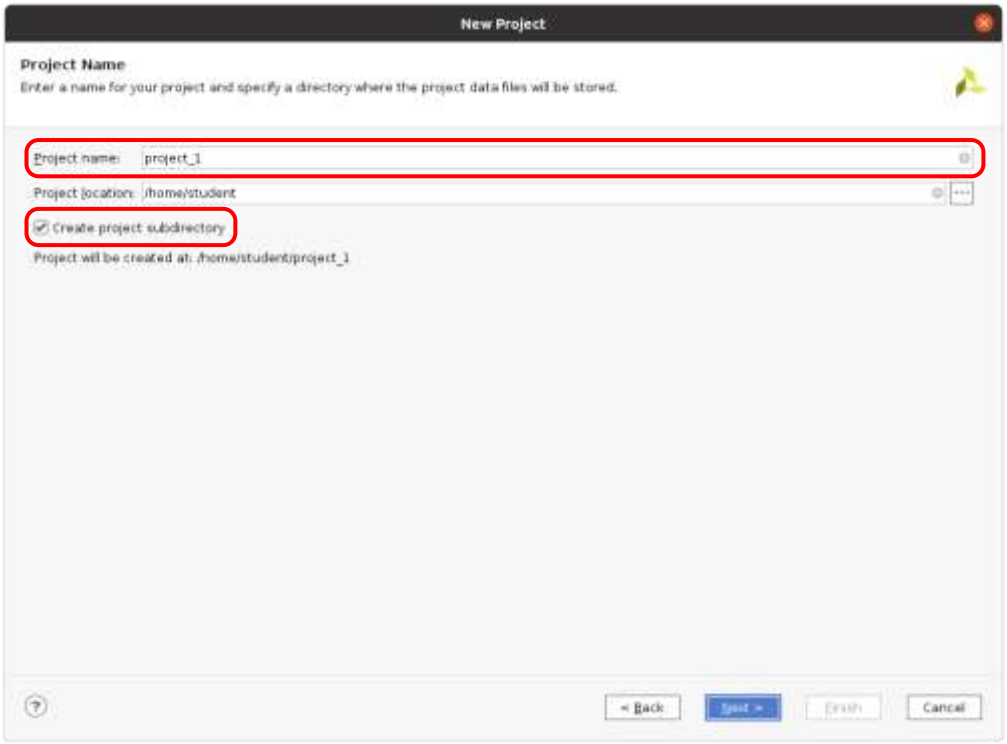


Figure 5: New Project wizard step 1 (Project Name)

Click **Next** to continue.

In step 2 (Project Type) keep the default selection *RTL Project* (Figure 6). Click **Next** to continue.

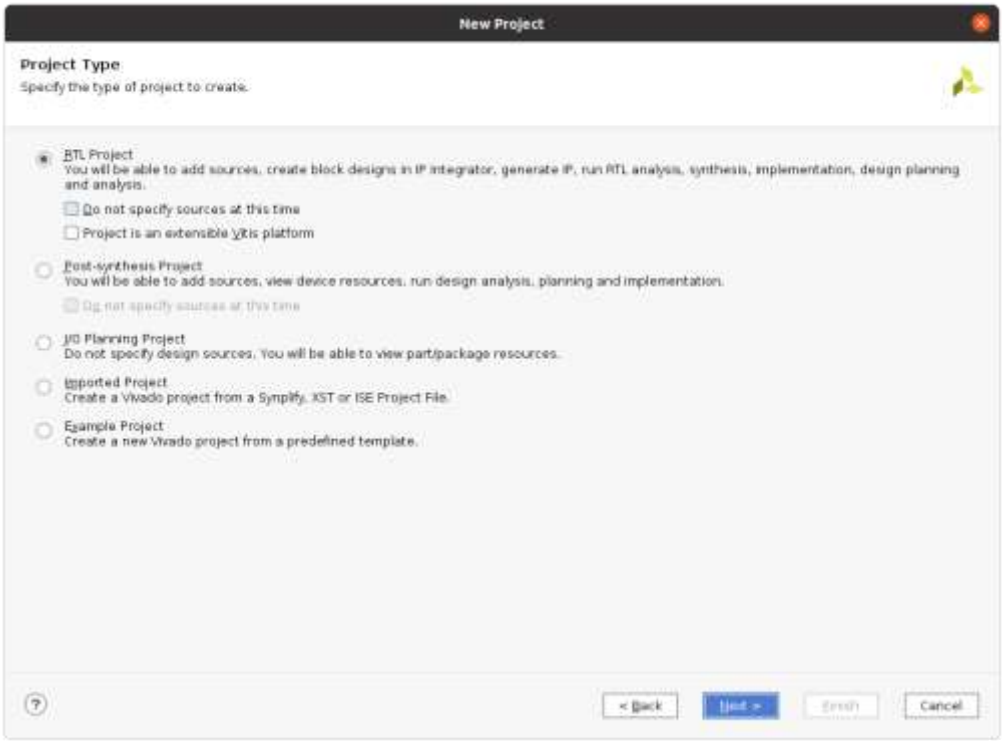


Figure 6: New Project wizard step 2 (Project Type)

In step 3 (Add Sources) you may add design source files or create new ones (Figure 7). You may add or create files anytime later (see section Create Source Files). Click **Next** to continue.

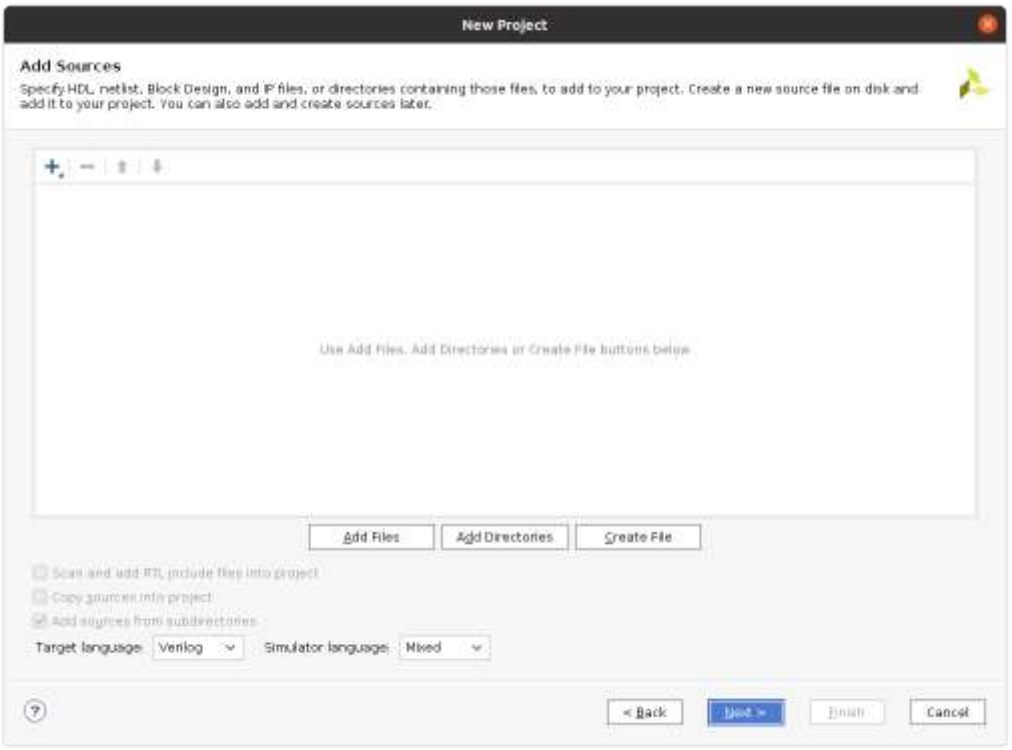


Figure 7: New Project wizard step 3 (Add Sources)

In step 4 (Add Constraints) you may add or create constraint files (Figure 8). You may add or create them anytime later. Click **Next** to continue.

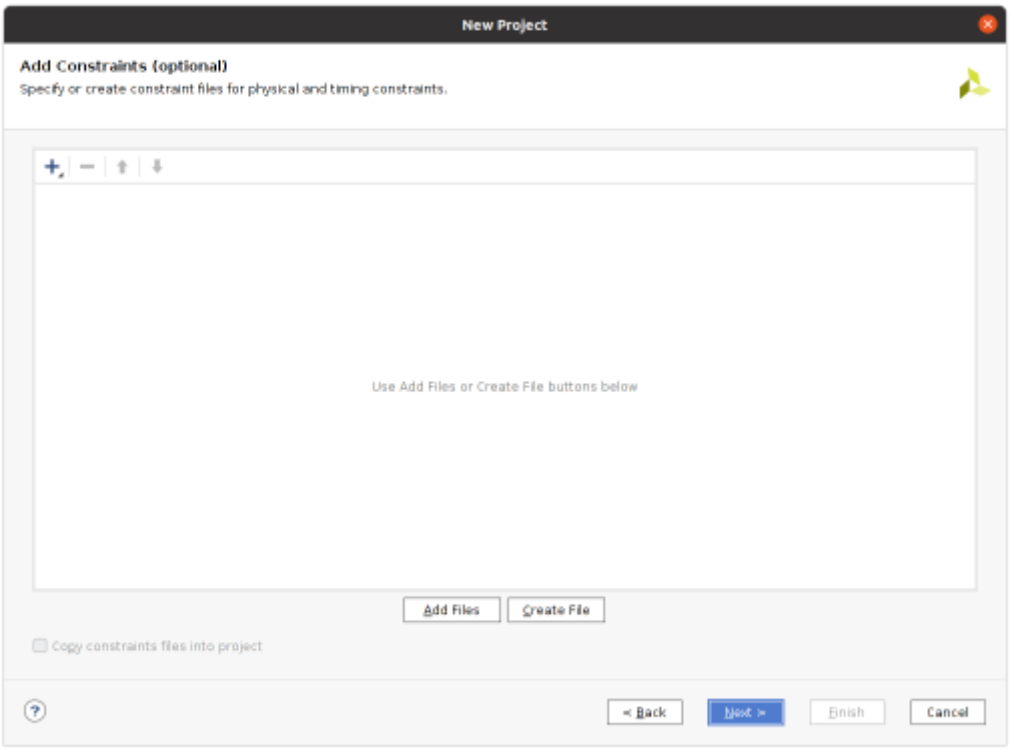


Figure 8: New Project wizard step 3 (Add Constraints)

In step 5 (Default Part) of the New Project wizard (Figure 9) change the tab from **Parts** to **Boards**.

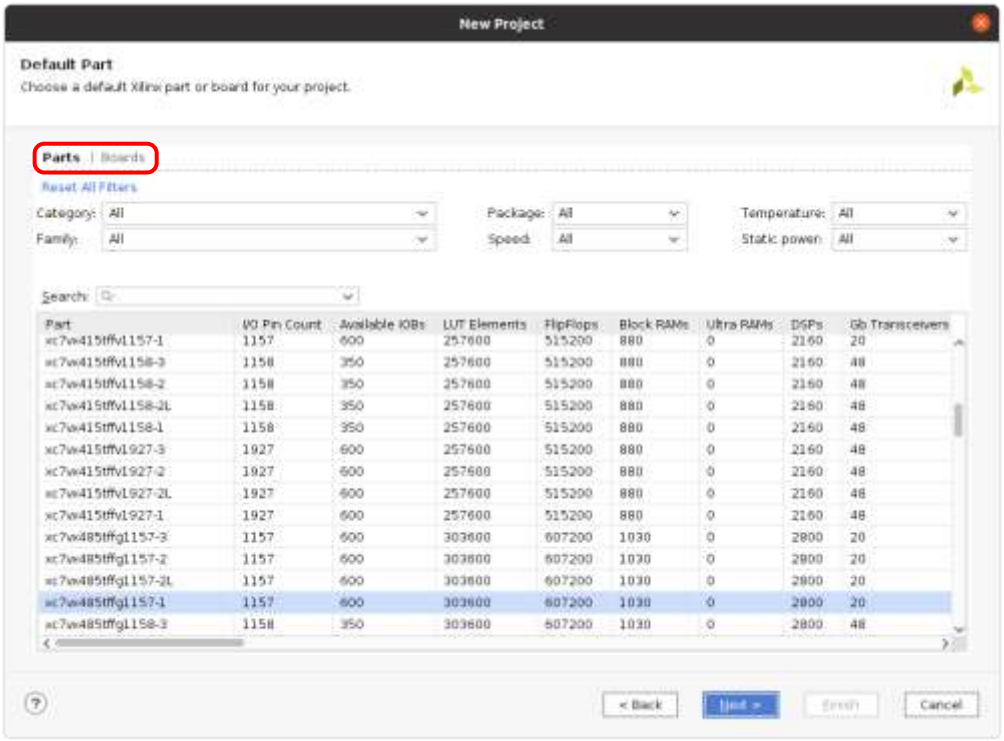


Figure 9: New Project wizard step 5 (Default Part)

Select the pynq-z2 board from the list of boards (Figure 10).

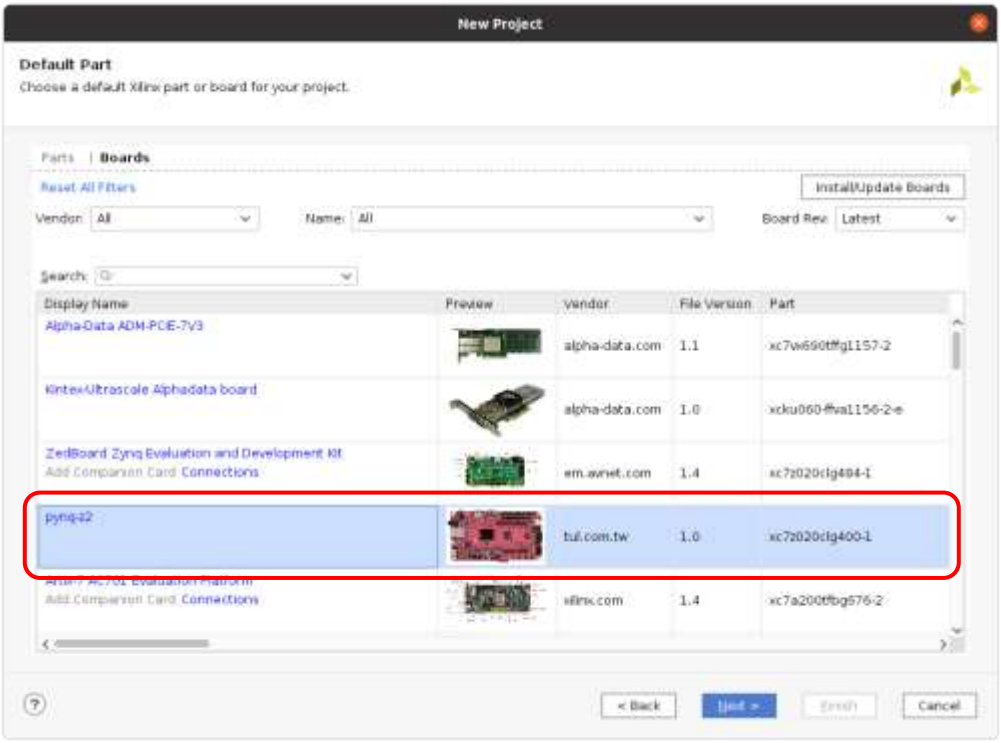


Figure 10: New Project wizard step 5 (Default Part) with the Pynq-Z2 board selected

After you selected the board click **Next**.

The last dialog of the New Project wizard (Figure 11) shows a brief description of the settings and selections you have made. Click **Finish**.

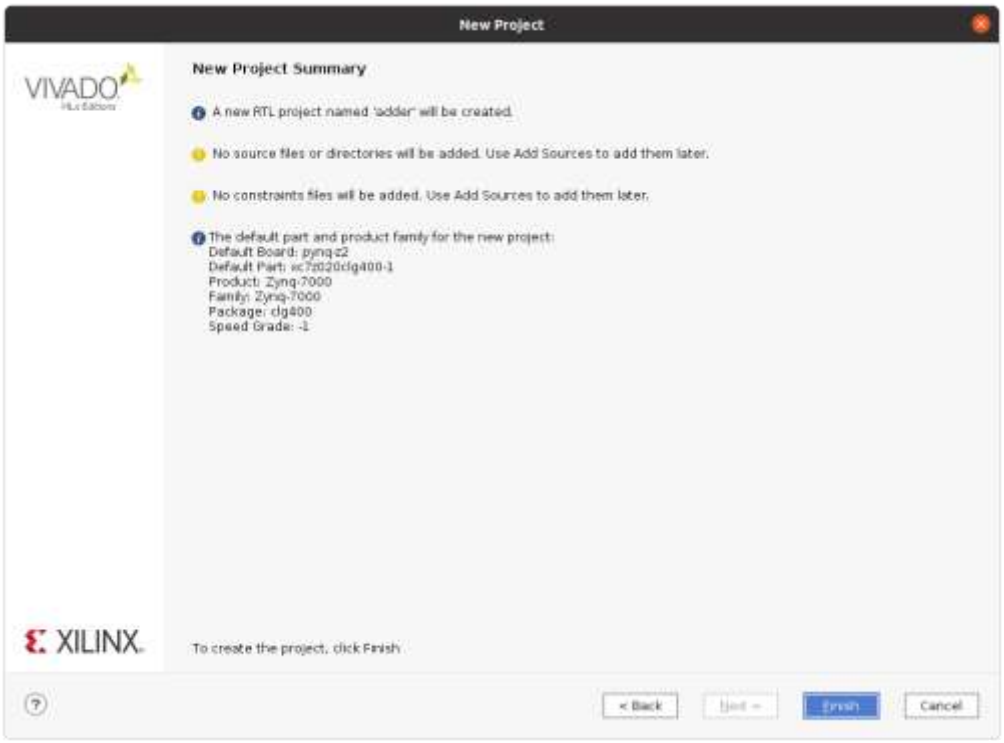


Figure 11: New Project wizard summary

After Vivado has created and initialized the project, it opens the Project Manager window (Figure 12).

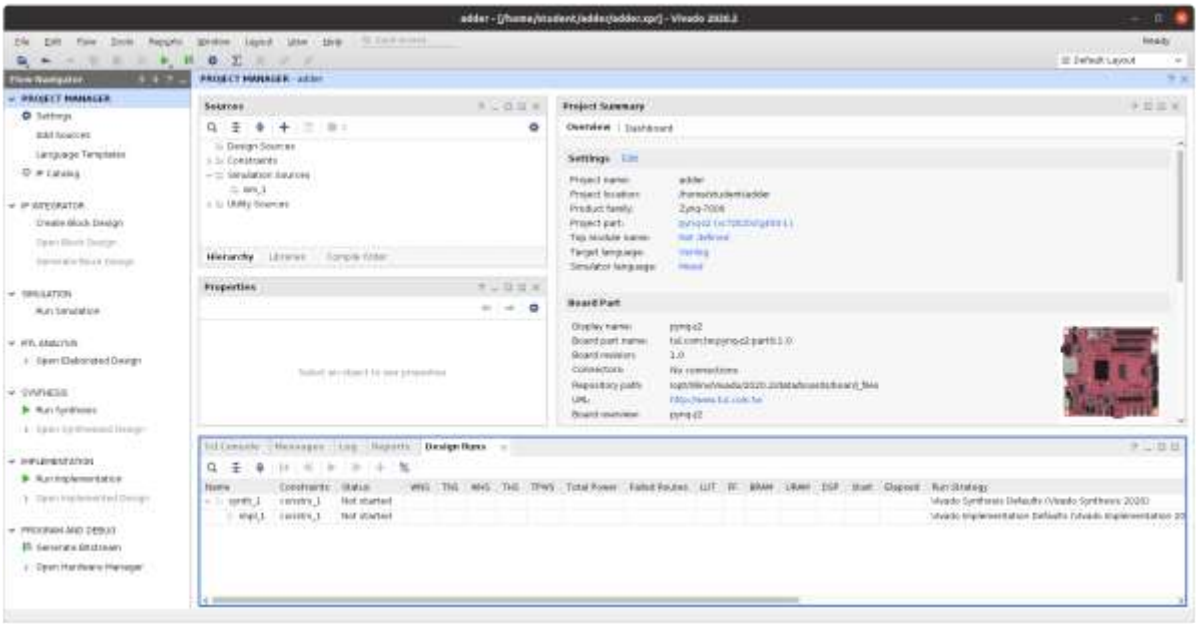


Figure 12: Vivado project manager window

Create Source Files

To create a new design source file, click on the 'Plus' button in the *Sources* panel (Figure 13) from the project manager window.

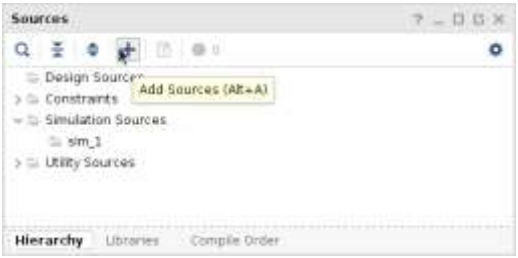


Figure 13: Open a new source file

In the *Add Sources* dialog window that opens (Figure 14), select the file type you want to create (design source, simulation source or constraints) and click **Next**.

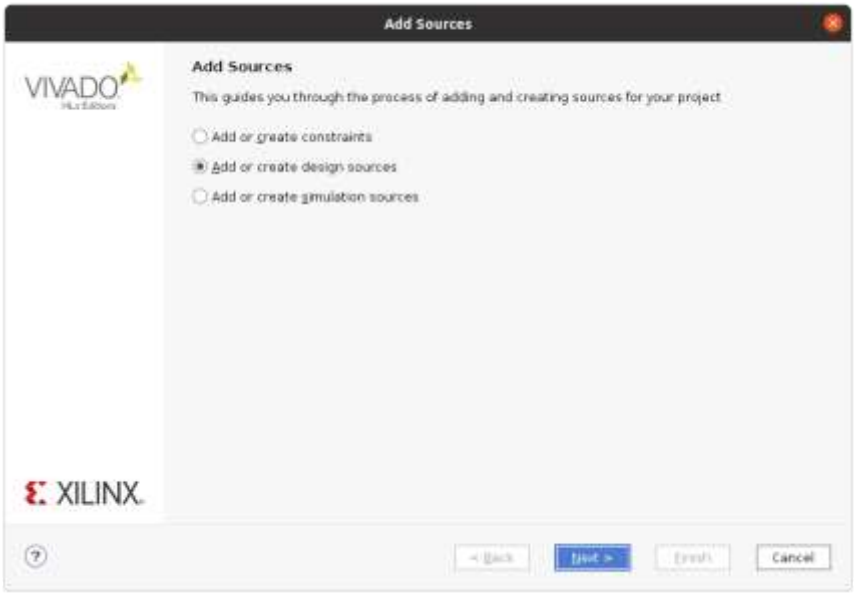


Figure 14: Source file type selection

Alternatively, in the *Sources* panel you may right click on the desired type you want to create (Design Sources, Constraints or Simulation Sources) and from the pop-up menu select the **Add Sources …** option (Figure 15).

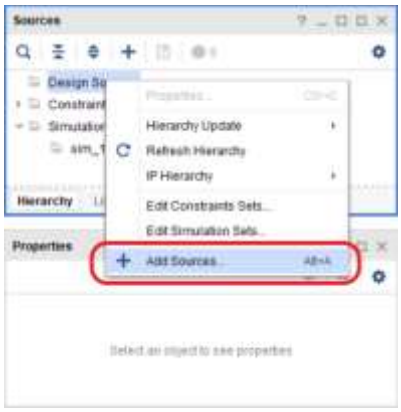


Figure 15: Open a new source file of the desired type

This alternative way opens the *Add Sources* dialog with the desired file type selected by default.

Click **Next**.

The next *Add Sources* dialog opens (Figure 16). You may add files to the project or create new ones. Click on **Create File** button.

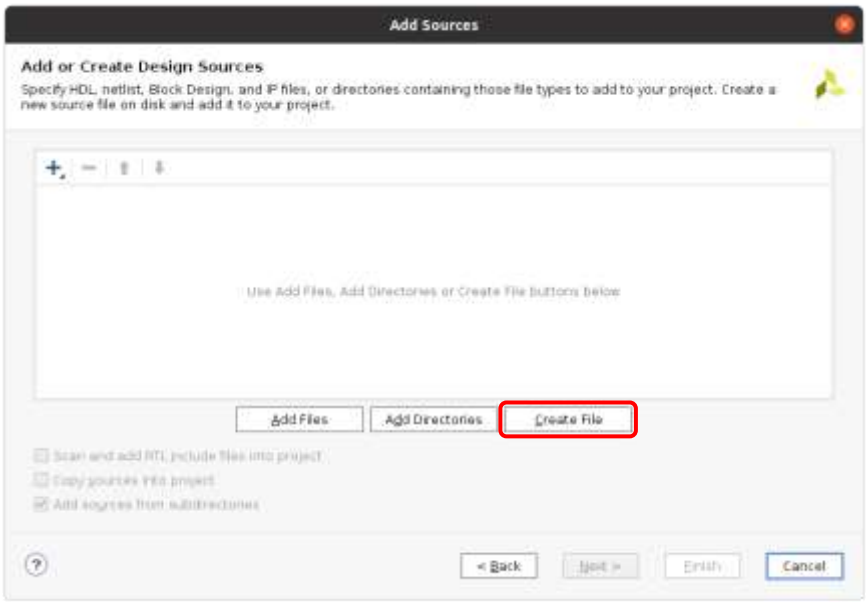


Figure 16: Add Sources window

In the small dialog box that opens (Figure 17) enter the desired name for the source file in the *File Name* text editor field, but keep unchanged the default values of *File Type* and *File Location*. Click **OK**.

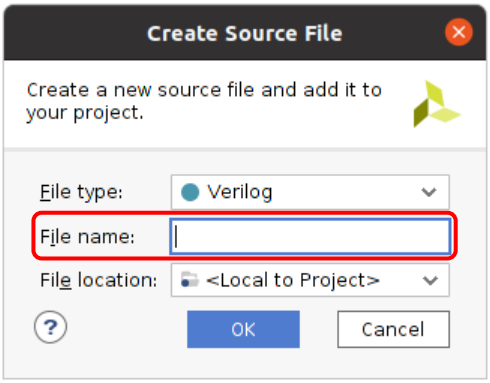


Figure 17: Enter the new file name

The new file is added to the list of files of your project (Figure 18).

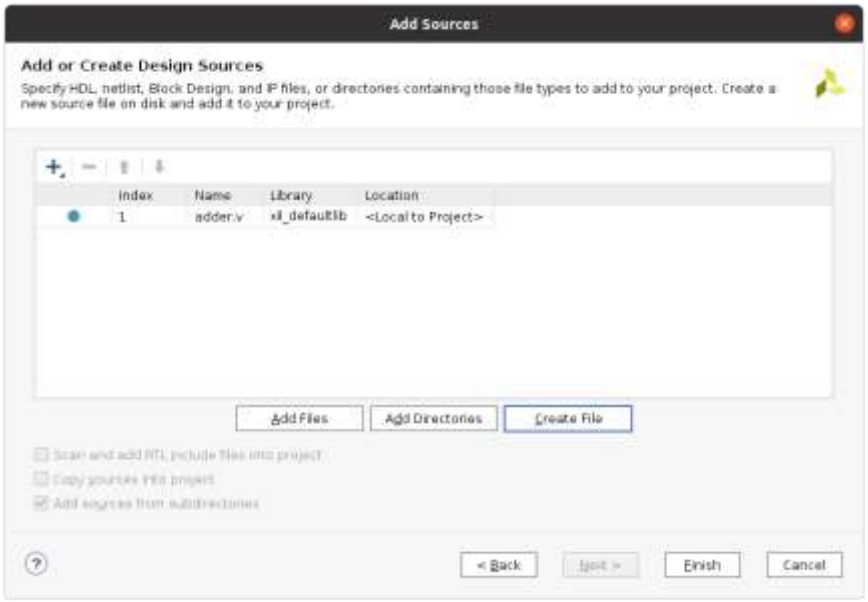


Figure 18: Add Sources window with the new file added to the list

After you added and created the desired files click **Finish**.

Immediately after design source file or simulation source file creation, Vivado opens another dialog window (Figure 19) that allows you to define the interface for each newly created Design Source and Simulation Source. You may skip this option by clicking **OK**.

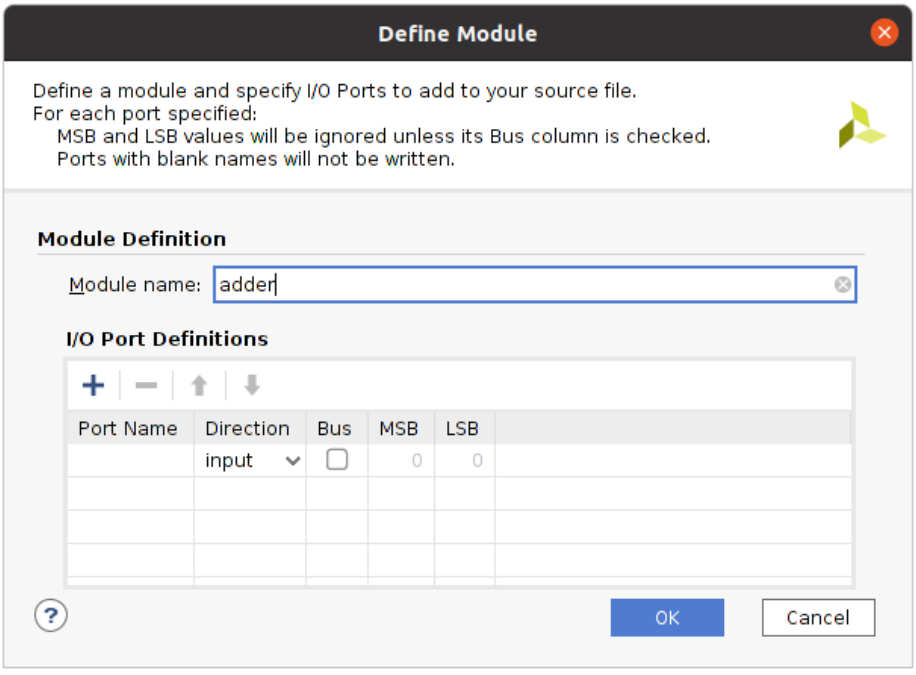


Figure 19: Define Module window

The interface of a module may be edited in the *I/O Port Definitions* table. For a single-bit port you should enter a *Port Name* and select its *Direction* (`input` by default). As an example, a newly created adder module is defined with 2 one-bit inputs `a` and `b`, and a third port, `c`, is declared as `output`. To change the *Direction*, click on the downward arrow and select the desired direction from the drop-down list (Figure 20).

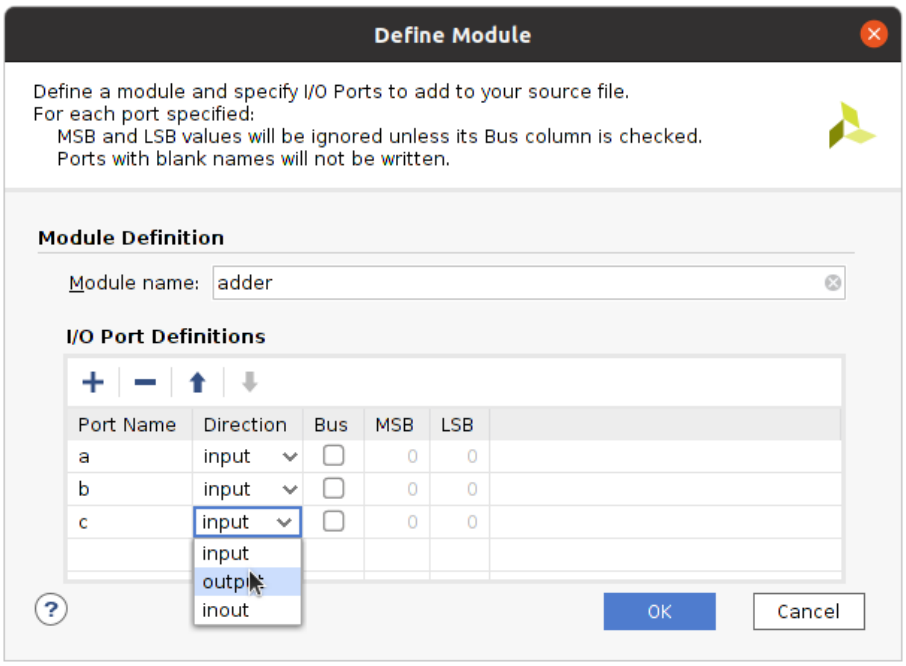


Figure 20: Define module window, change a port direction

Some ports may have more than one bit. They may be defined by checking the *Bus* checkbox and entering the *MSB* and *LSB* values. *LSB* should be 0. *MSB* is equal to the desired width minus 1. The MSB and LSB values (default values are 0) may be changed by editing the *MSB* and *LSB* textbox or using the up and down arrows to increment or decrement the value.

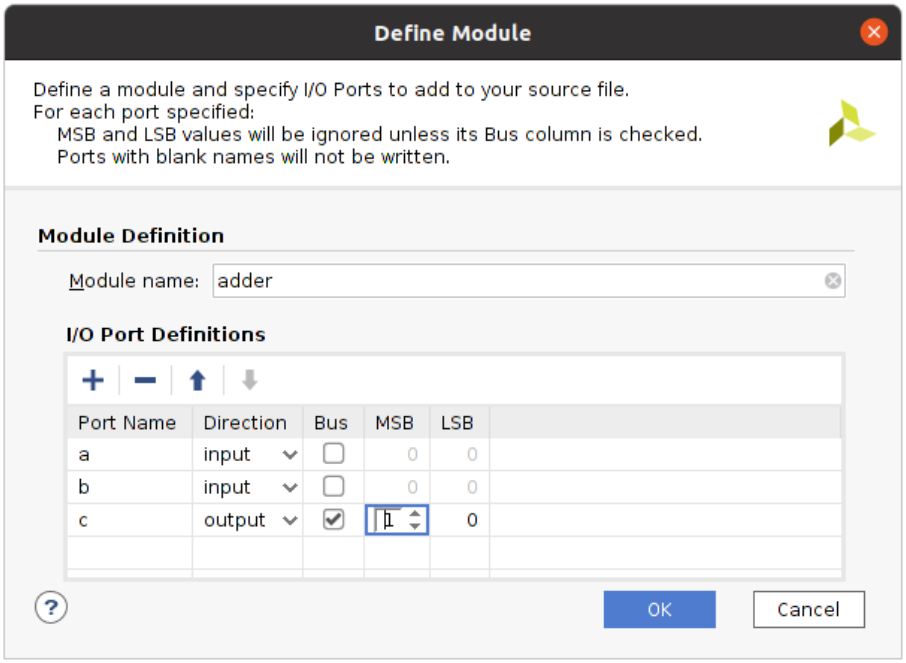


Figure 21: Define module window, change a port width

Click **OK**. To finish file creation.

- **Each module is in a separate source file.**
- **The name of the source file is the name of the module.**
- **Keep the default file location for any created file.**
- **The top-level module name and its source file name must match the name of the project.**

Add Source Files

If you want to include in your project a file that is already on your computer open the *Add Sources* window as shown in the previous section and click **Add Files** button (Figure 22):

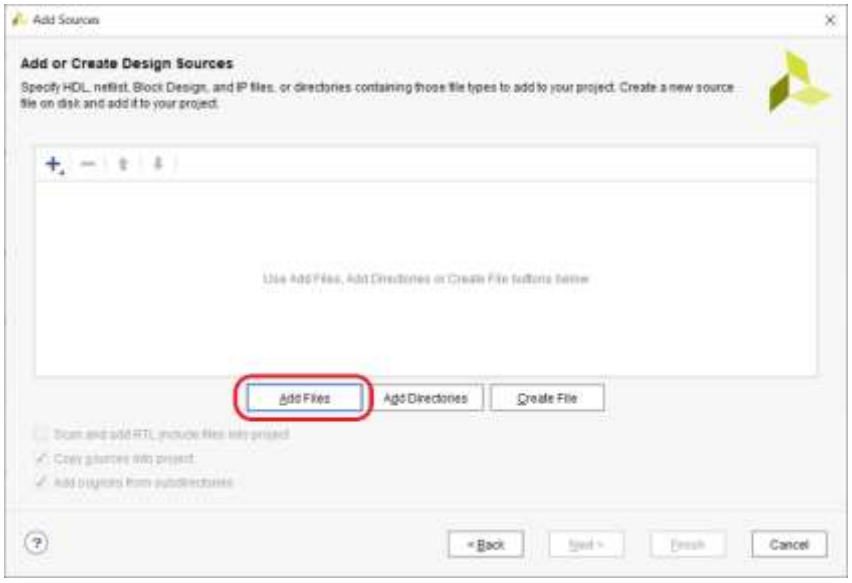


Figure 22: Add Sources window.

A file browser opens (Figure 23). Use the 'Up' button (encircled in red) to go up in the file hierarchy and click on folder names in the left panel to go down in the file hierarchy. Select the files you want to copy into the project and click **OK**.

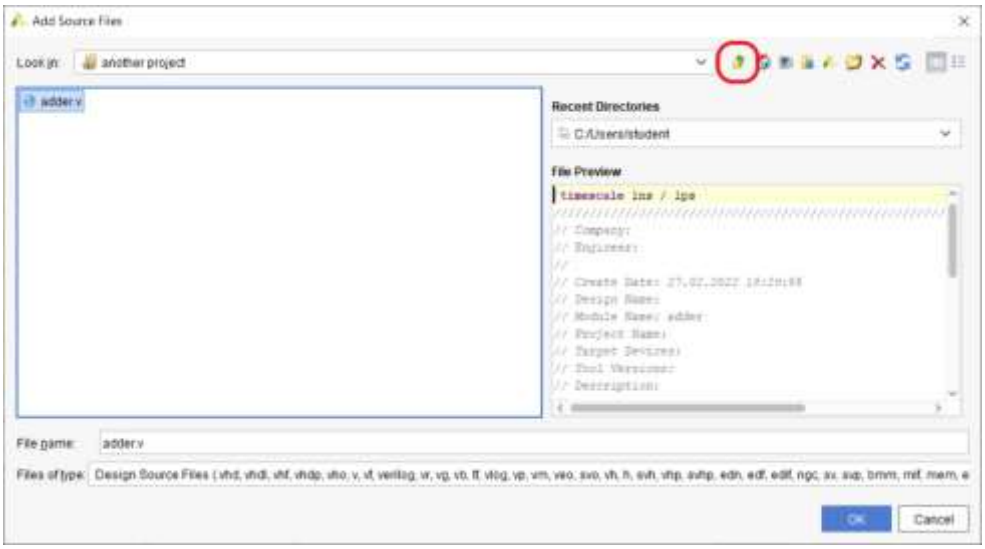


Figure 23: Add Source File browser

The selected files are added to the list of project files in the *Add Sources* window (Figure 24). You should check the *Copy sources into project* checkbox. Click **Finish**.

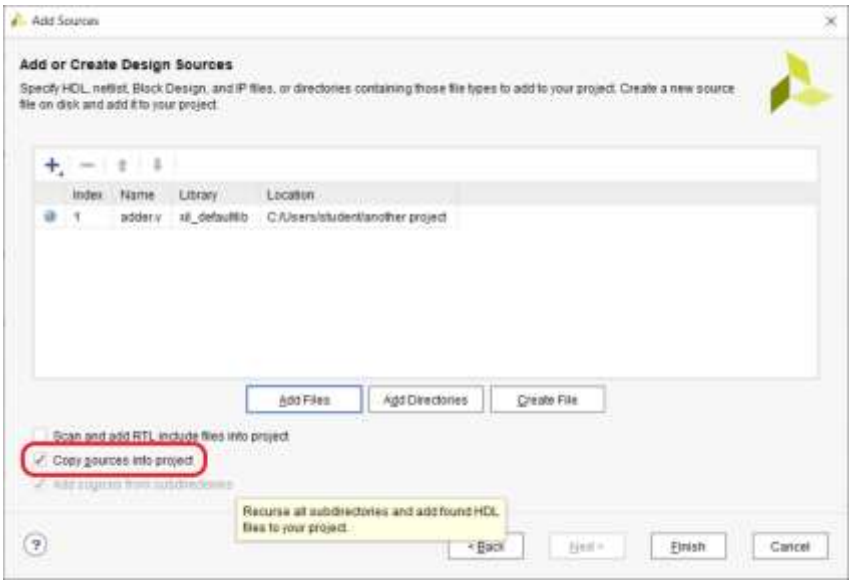


Figure 24: Add Sources window

- **Make sure that any added file is also copied into project.**

Source File Editor

To open a file for editing double click the file in the *Sources* panel. The editor window (Figure 25) opens in another tab of the rightmost panel of the Vivado Project window. You may edit all the file.

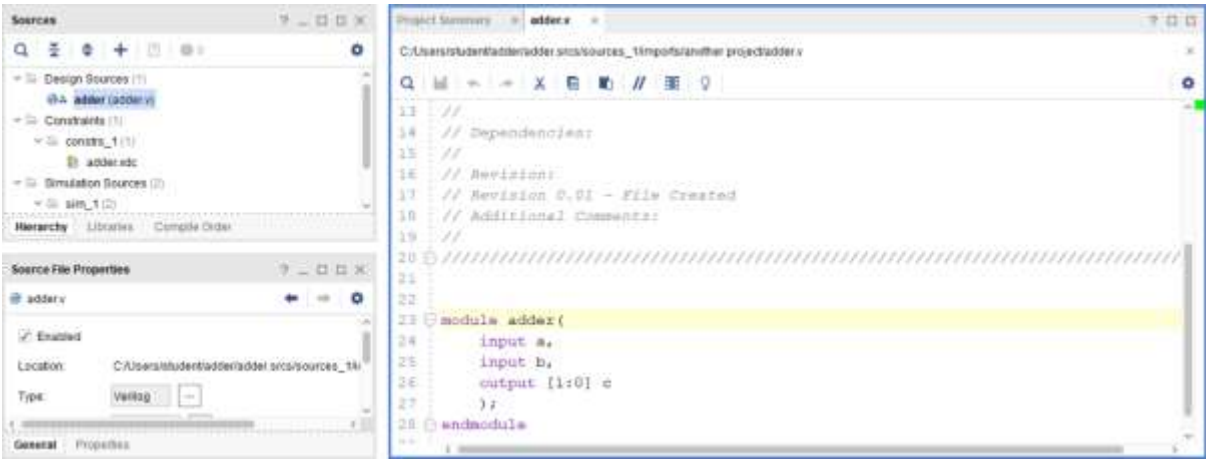


Figure 25: File editor window

To save the file click on the 'Save' icon at the top row of the editor window. After a file is changed and saved, Vivado updates the hierarchy of modules in the *Sources* panel (this takes a few seconds).

Simulation

On the left panel *Flow Navigator* expand the SIMULATION section and click on **Run Simulation**. From the pop-up menu list select **Run Behavioral Simulation**. Vivado starts the elaboration of the design. This takes some time while a dialog shows the progress of this compilation:

If the elaboration succeeds, Vivado opens the Simulation window (Figure 26).

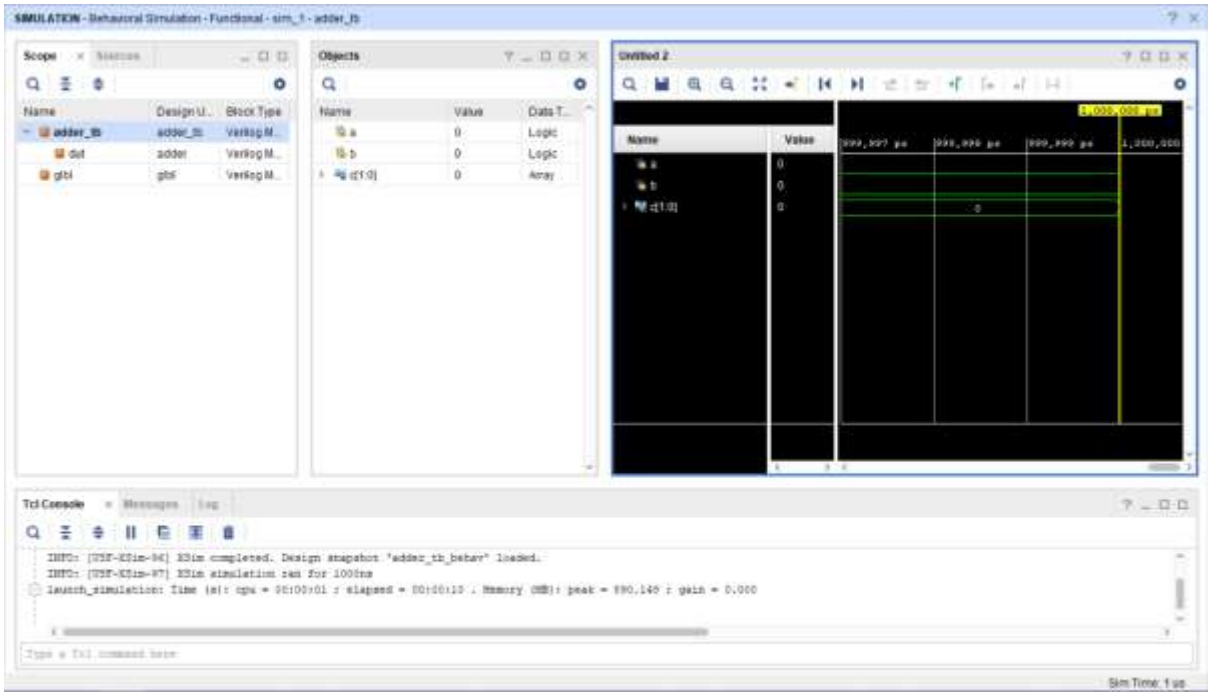


Figure 26: Vivado Simulation window

The Simulation window has four panels. The leftmost *Scope* panel shows the hierarchy of the modules instantiated in your project, with the testbench module at the root of the hierarchy. The middle *Objects* panel lists all signals for the module that is selected in the *Scope* hierarchy. The rightmost panel draws the waveforms of the signals chosen to be displayed. By default the Simulation window opens with the testbench module selected and with all its signals been displayed on the waveform panel.

The bottom panel (*Transcript* panel) reports messages from Vivado and logs everything displayed by the simulated modules themselves.

The most important controls of the simulation are the **Restart**, **Run All** and **Relaunch Simulation**. They are available from Vivado main menu **Run** section but are easier to choose from Vivado toolbar (Figure 27).

Figure 27: Vivado Simulation controls

The Wave window may be arranged to suit your needs. You may rearrange the signals by clicking a signal name and dragging it up or down in the list. You may shrink or expand the time scale using the **Zoom In**, **Zoom Out** and **Zoom Fit** icons of the Wave window's toolbar (Figure 28).

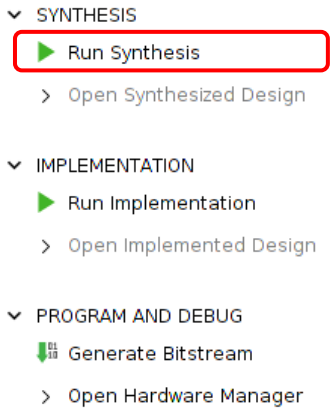
Figure 28: Wave window main controls

Note: If there are no signals in the Wave and Object windows, that means the testbench has not compiled because of compiling errors, or it has not loaded because the module it instantiates does not match the compiled top-level design module (the interface is different, or the module name does not match). In the *Scope* panel at the left of the Simulation window you will see some instances, but not the testbench instance. In that case you must look for the errors in the *Transcript* panel at the bottom of the simulation window, close the simulator, fix the errors in the testbench, and then relaunch the simulator.

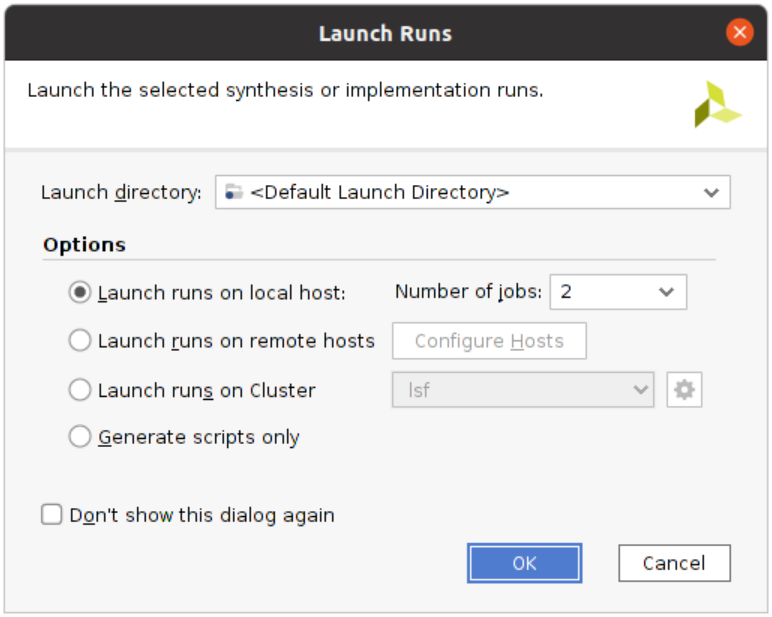
I/O Ports Assignment

Synthesis and Implementation

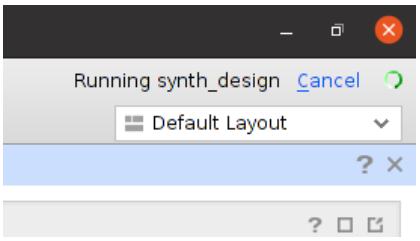
On *Flow Navigator* panel expand the SYNTHESIS section and click on **Run Synthesis**.



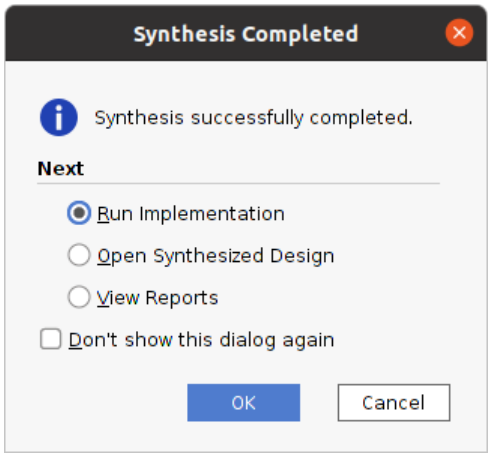
In the dialog window that appears keep all default settings and click **OK**.



The synthesis takes some time to complete (between tens of seconds and tens of minutes, depending on the design complexity and constraints). While it is running the message `Running synth_design` appears at the top-right corner of the main program window:

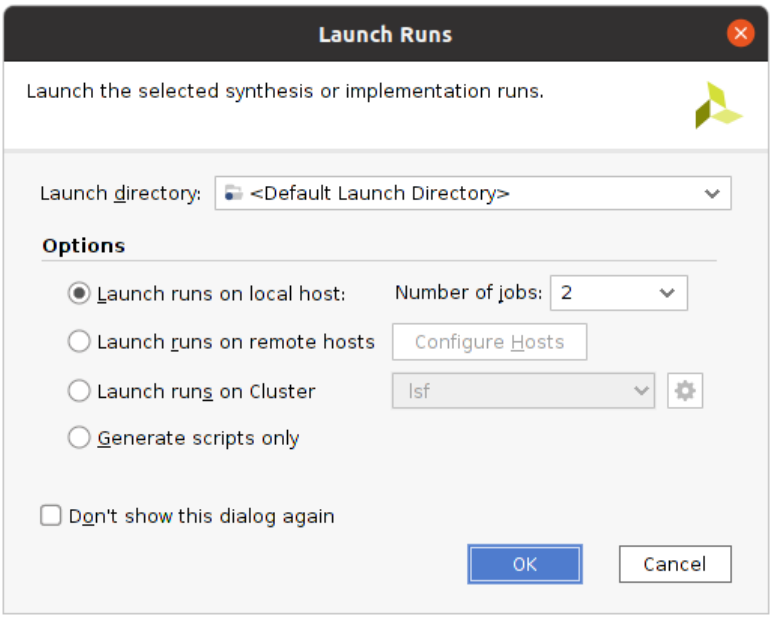


When the synthesis finishes a dialog window appears:

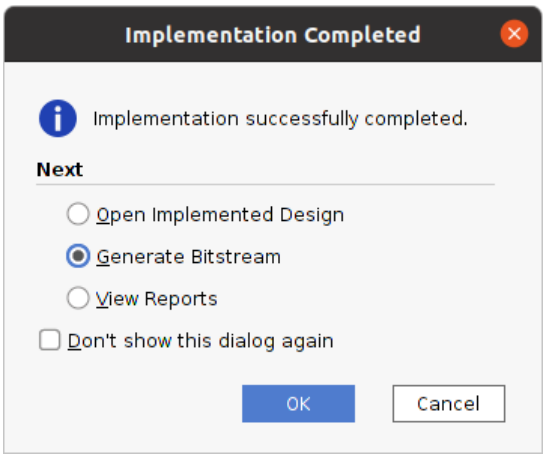


Keep the default choice (*Run Implementation*) and click **OK**.

In the new dialog window that appears keep all default settings and click **OK**.

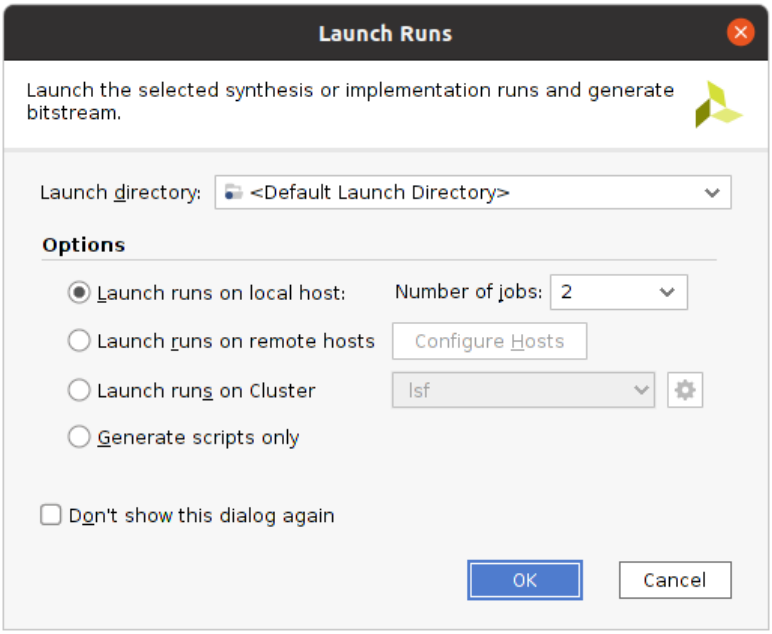


The implementation is also a time-consuming process, even more so than the synthesis. While it is running a info message appears at the top-right corner of the program's main window. If the implementation finishes without errors a dialog window opens:

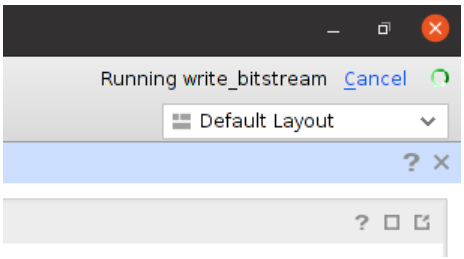


Keep the default choice (Generate Bitstream) and click **OK**.

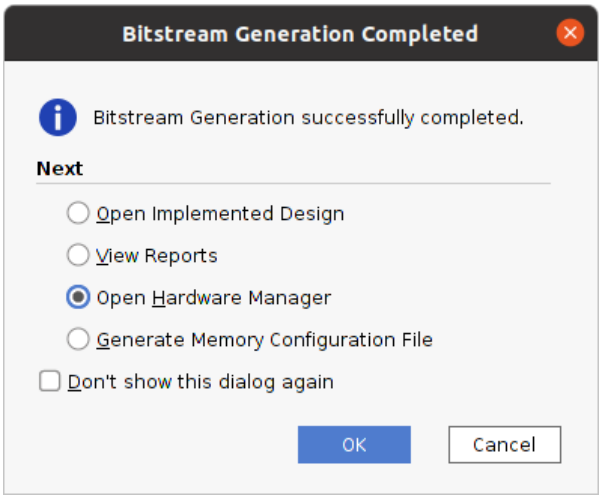
In the dialog window that appears keep all default settings and click **OK**.



The bitstream generation also takes some time, while an info message is displayed at the top-right corner of the program main window:



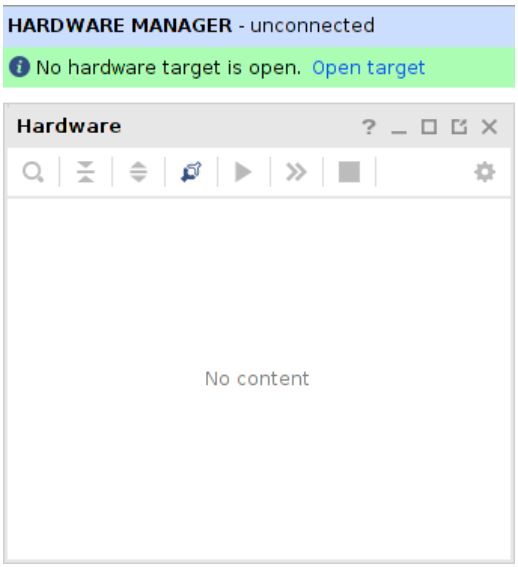
If the bitstream generation finishes without errors, another dialog window opens up:



Keep the default choice (Open Hardware Manager) and click **OK**.

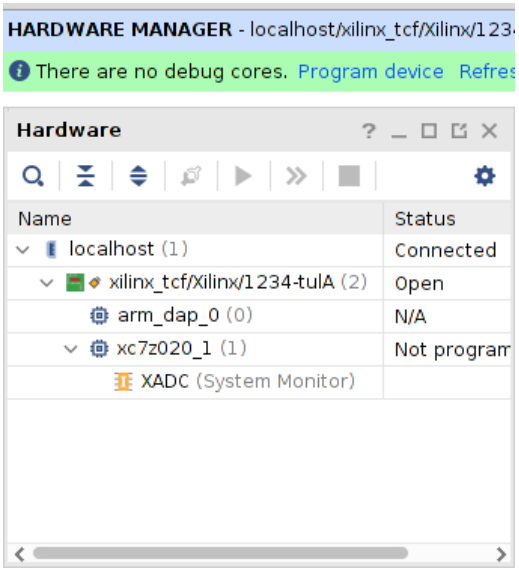
Device Programming

If the board is not powered up the following message appears above the central panel:

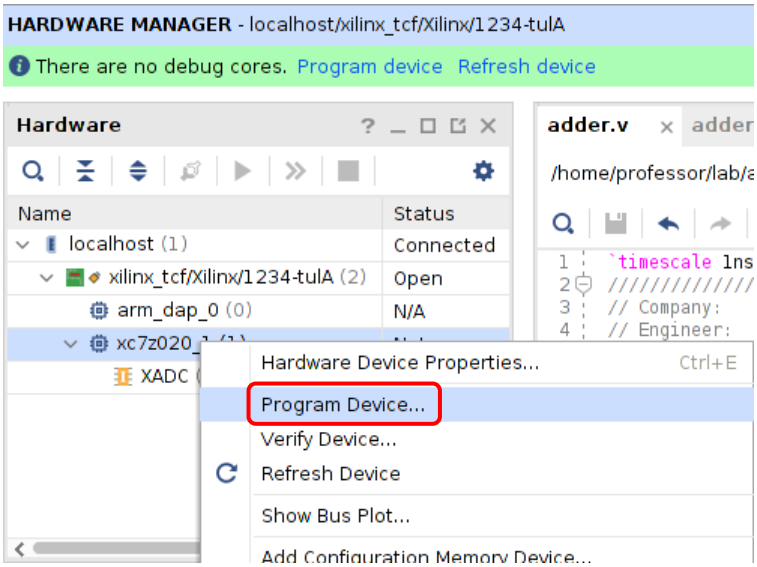


Power-up the Pynq-Z2 board, then click **Open target**. From the drop-down menu click on **Auto Connect**:

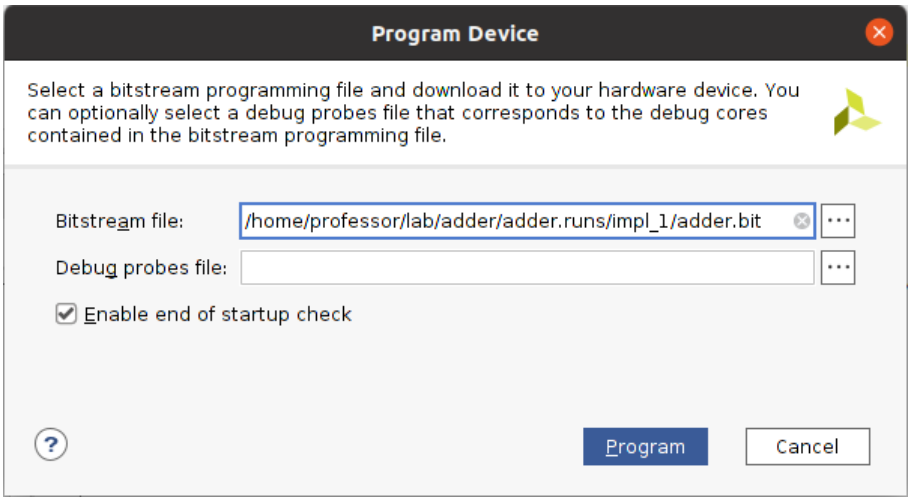
If the board is power-up and connected to the computer, the following list appears in the Hardware panel:



It shows that the localhost (your computer) is connected to a Xilinx chip which has an ARM processor and an FPGA. Click on the FPGA **xc7z020** and in the pop-up window that shows-up click on **Program Device …**



A dialog window appears, allowing you to select the bitstream file to be written into the target device. If you followed the above default steps, keep the default *Bitstream file* selection and click **Program**.



If the target device (the FPGA or the board) was correctly set up during the project initialization, the bitstream could be written into the FPGA, and the PL programming “done” LED should be on.

Your project is ready to use.

Quick Project Guide

- **New Project** wizard
  - Step 1 (Project Name)
    - **Project name**: *myProject*
    - Check *Create project subdirectory* checkbox
  - Step 2 (Project Type)
    - Select *RTL Project*
  - Step 3 (Add Sources)
    - Skip this step: Select **OK**
  - Step 4 (Add Constraints)
    - Skip this step: Select **OK**
  - Step 5 (Default Part)
    - Change tab to **Boards**
    - From Boards list select the *pynq-z2* board
- Create source files
  - Click 'Plus' on *Sources* panel
  - Choose file type, then **Next**
  - Click **Create File** on *Add Sources* dialog, then **Next**
  - Click **Finish** in the *Add Sources* dialog
  - Optionally edit the interface. Otherwise let it unfilled and click **OK**.
- Add source files
  - Click 'Plus' on *Sources* panel
  - Choose file type, then **Next**
  - Click **Add File** on *Add Sources* dialog
  - Select the desired file, then **OK**
  - Click **Finish** in the *Add Sources* dialog
- *Flow Navigator* -> SIMULATION -> **Run Simulation** -> **Run Behavioral Simulation**
- *Flow Navigator* -> SYNTHESIS -> **Run Synthesis**
- *Flow Navigator* -> IMPLEMENTATION -> **Run Implementation**
- *Flow Navigator* -> PROGRAM AND DEBUG -> **Generate Bitstream**
- *Flow Navigator* -> PROGRAM AND DEBUG -> **Open Hardware Manager**
  - Power on the physical board (the 'power on' red LED should be on)
  - *Open target* -> **Auto Connect**
  - XC7Z020 -> **Program Device …**
  - Keep the default *Bitstream file* name and click **Program**