ELECTRONIC DEVICES AND CIRCUITS II

Mod. MCM4/EV

Volume 1/2

THEORY AND EXPERIMENTS

TEACHER / STUDENT manual

ElettronicaVeneta

"Final English version provided by cambridge Open Learning"

CONTENTS

SAFETY RULES

Keep this handbook at hand for any further help.

After the packaging has been removed, set all accessories in order so that they are not lost and check the equipment integrity. In particular, check that it shows no visible damage.

Before connecting the equipment to the +/- 12V power supply, be sure that the rating corresponds to the one of the power mains.

This equipment must be employed only for the use it has been conceived, i.e. as educational equipment, and must be used under the direct supervision of expert personnel.

Any other use is not proper and therefore dangerous. The manufacturer cannot be held responsible for eventual damages due to inappropriate, wrong or unreasonable use.

LESSON B13: NPN and PNP TRANSISTORS

OBJECTIVES

- To identify PNP and NPN transistors
- To measure the interjunction resistances
- To use an ohmmeter to identify the three terminals: Base, Emitter, Collector
- To check the relationships beteween the main dc parameters
- To measure the collector current variation with base current
- To calculate the amplification factors α and β

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod.MU/EV), Individual control unit mod. SIS1/SIS2/SIS3 (optional)
- **The module may work in a stand-alone mode, the faults are inserted via the on-board DIP switches: When using the external management units, the 4 left DIP switches must be in the "ON" position, and the 4 right DIP switches must be in the "OFF" position.**
- experiment module mod.MCM4/EV
- multimeter

B13.1 BASIC THEORY
PNP and NPN structures

The models of transistors PNP and NPN are shown in figure B13.1. The central region is called the "Base" while the outer regions are known as the "Emitter" and "Collector".

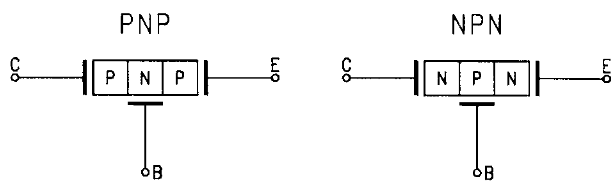


fig. B13.1

The operation is based on the ability to control the current between the Collector and Emitter by a small current into the base B. This is obtained by a forward bias on the base-emitter and a reverse bias on the base-collector. With no bias voltages, the potential barriers are as shown in the figures.

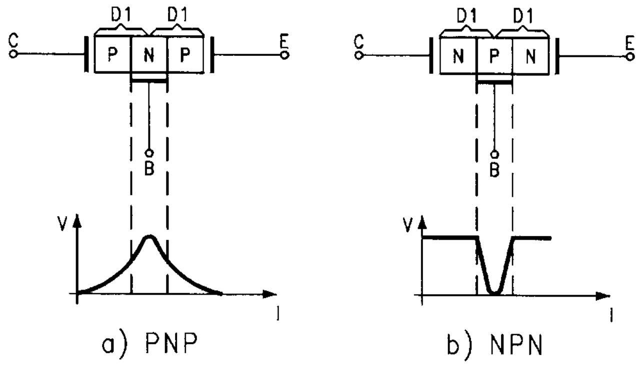


fig. B13.2

PNP transistor operation

In normal operation, the base-emitter diode D_2 is forward biased (positive on the emitter and negative on the base). The collector-base diode D_1, though is reverse biased with the collector at a negative potential with respect to the base (figure B13.3a).

With the base-collector circuit open (figure B13.3b), as the diode D_2 is forward biased, its potential barrier decreases. This allows the positive carriers to move from the emitter to the base.

Now, consider a situation in which the collector-base circuit is closed and the base-emitter is open (figure B13.3c). The reverse biasing makes the potential barrier of the collector-base diode increase. So, only a small current flows from the base to the collector.

Now, suppose both the base-emitter and the collector-base circuits to be simultaneously closed (figure B13.3d). The base thickness is very thin compared to the average distance moved by the positive holes coming from the emitter, so a considerable number of these carriers can cross over and reach the collector-base junction. Here they will be attracted by the collector negative potential, so producing an emitter-collector current.

For NPN transistors (figure B13.4), a similar explanation and operation applies, but the voltages and currents are reversed compared to an NPN.

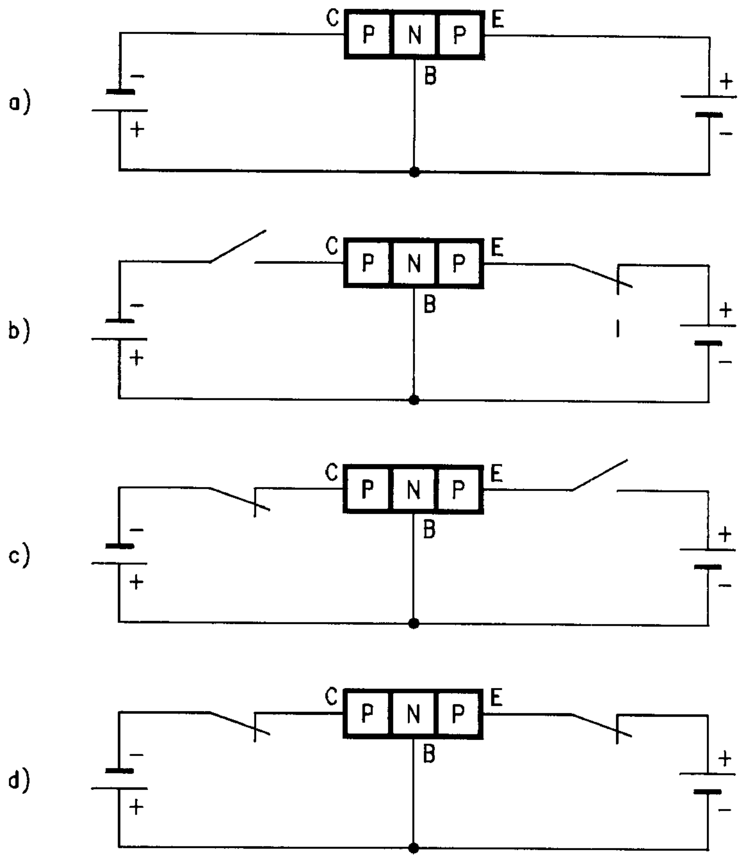


Fig. B13.3

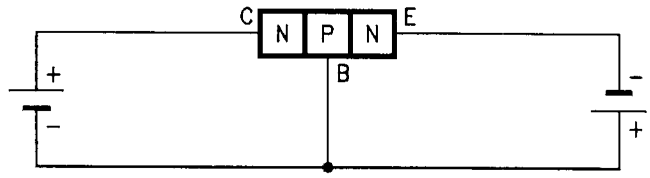


Fig. B13.4

The PNP and NPN structures are the two types of bipolar transistors or "BJT" (Bipolar Junction Transistor).

Their symbols are as shown.

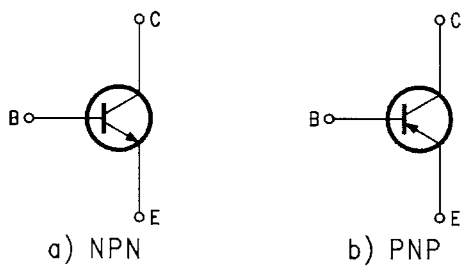


fig. B13.5

The arrow shows the direction of conventional current for the emitter. Figure B13.6 shows the correct biasing for a BJT.

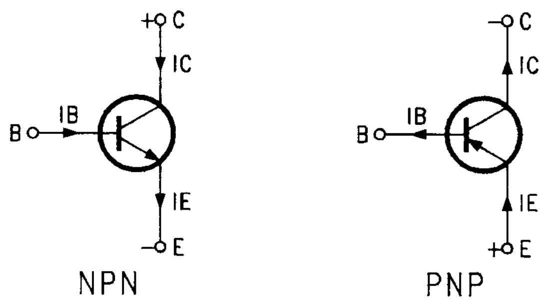


fig. B13.6

In the case of DC, the variables that determine the operation of a transistor are (figure B13.7):

1. the three currents through the transistor (I_B, I_C, I_E)
2. the three voltages present across the terminals (V_{BE}, V_{CE}, V_{CB})
3. the two current amplification coefficients (α, β)

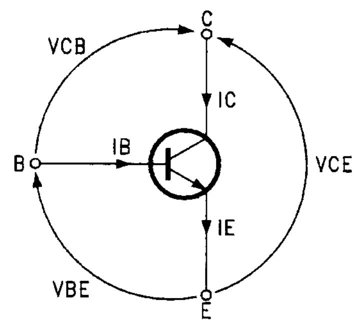


fig. B13.7

Basic equations

Taking the conventional current direction as that of positive carriers, the following equations apply:

$$I_E = I_C + I_B \qquad \text{B13.1}$$

$$I_C = \alpha \cdot I_E + I_{CBO} \qquad \text{B13.2}$$

where:

- the coefficient α is between 0.9 and 0.999

- $\alpha \cdot I_E$ indicates the fraction of the emitter current reaching the collector (and α is almost equal to 1.0)
- I_{CBO}, in the order of nA, is the (reverse) current in the reverse biased base-collector junction. It is measured with the emitter terminal open

The following equation is obtained by substituting I_E from B13.1, into B13.2:

$$I_C = \beta \cdot I_B + I_{CEO} \qquad \text{B13.3}$$

where:

$$\beta = \alpha/(1-\alpha) \qquad \text{B13.4}$$

$$I_{CEO} = (\beta+1) \cdot I_{CBO} \qquad \text{B13.5}$$

From B13.4, using typical values of α you obtain the values of β ranging between 10 and 100. From these equations, you can note that a small current, I_B in the base corresponds to a high current I_C , in the collector. This indicates that the transistor is a current amplifier. For the voltages we have :

$$V_{CE} = V_{BE} + V_{CB} \qquad \text{B13.6}$$

Static gain of the transistor

The following equation for β can be obtained from equations B13.3 and B13.5:

$$\beta = \frac{I_C - I_{CBO}}{I_B + I_{CBO}} \qquad \text{B13.7}$$

Ignoring the small contribution of I_{CBO} in the numerator and denominator of B13.7, the static current gain h_{FE} - the most important parameter of the BJT can be found :

$$\mathbf{h_{FE} = I_C / I_B} \qquad \text{B13.8}$$

Characteristic curves

The last equations can be plotted on a graph, to give the characteristic curves shown in figure B13.8.

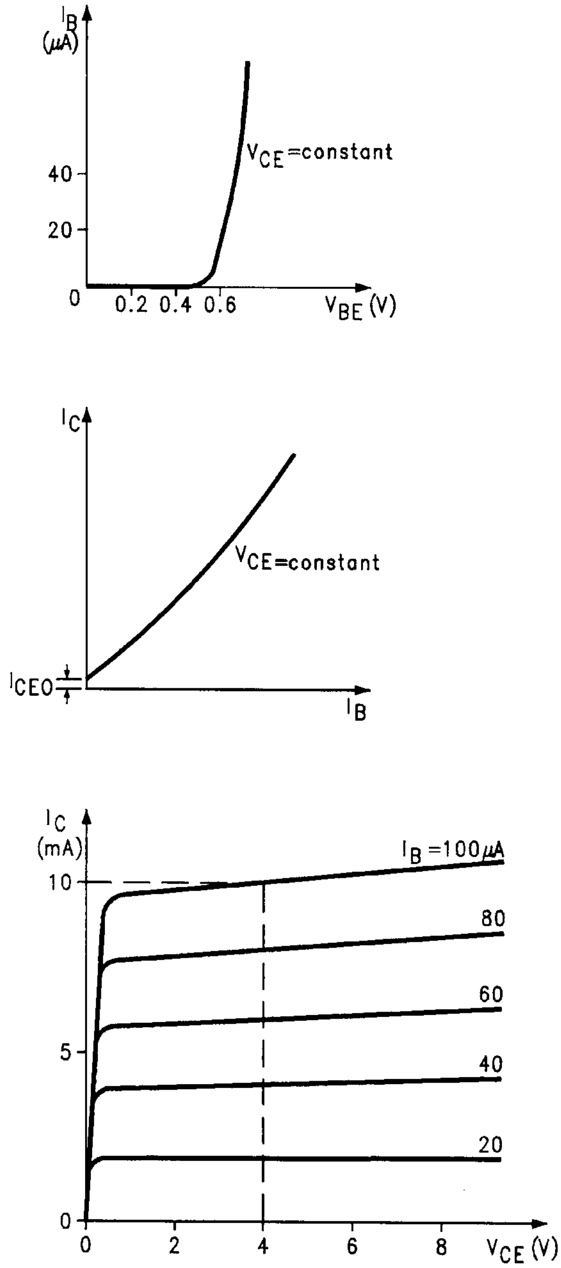


fig. B13.8   *a.*   *input characteristic of NPN, common emitter transistor*
b.   *transfer characteristic of NPN, common emitter transistor*
c.   *output characteristic of NPN, common emitter transistor*

B13.2 EXERCISES

➲ ***MCM4***	**Disconnect all jumpers**
➲ ***on-board SIS1***	**Turn all switches *OFF***
➲ ***SIS2***	**Insert lesson code: B13**

Voltage and current measurements will be required on some circuits. If only a single multimeter is available, this will be used sometimes as a voltmeter or at other times as ammeter. When used as a voltmeter, remember to short-circuit the points of the circuit where the ammeter would be inserted.

PNP or NPN identification

You may need to check the polarity of your ohm-meter: the output lines are sometimes reversed from their normal polarity when used to measure resistance.

- determine which pins correspond to the Base, Emitter and Collector of transistors T2 and T3
- set the ohmmeter to the lowest range. Measure the junction resistance between base-emitter, base-collector and collector-emitter in both directions. Compare the measured values with those in the next table:

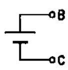
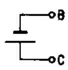
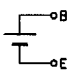
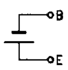
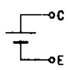
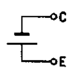
	R_{BC}		R_{BE}		R_{CE}	
						
T_2	low	∞	low	∞	∞	∞
T_3	∞	low	∞	low	∞	∞

fig. B13.9

- With the obtained resistance values, check that the transistor T2 is an NPN and that the transistor T3 is a PNP

Q1 *What is a simple representation of a transistor ?*

SET

A	*B*	
1	2	as two diodes in series, but in opposite directions, with base mid-point
2	4	as two diodes in parallel
3	1	as a normal diode and a Zener diode in series
4	5	with two diodes mounted in antiparallel
5	3	none of the above

Note that the pins of a transistor can be identified with this method.

Note also that the actual resistances can vary quite widely, even for BJTs from the same batch.

Experimental determination of the current relationships

- Set the variable power supply Vcc (Sez. (S5)) to +12V. Connect jumpers J2, J8, J6; insert the ammeters to produce the circuit of figure B13.10.

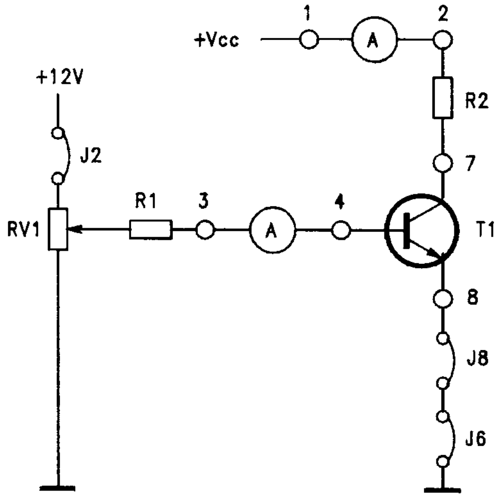


fig.B13.10

- measure the collector current I_C for the base current values I_B in the next table.

I_B (μA)	10	30	50	70	90
I_C (mA)					
h_{FE}					

- Plot the curve $I_C = f(I_B)$. I_B is the horizontal axis. The curve $I_C = f(I_B)$ is partly linear. Its slope gives the value of the static current gain, represented by

$$h_{FE} = I_C / I_B$$

- calculate the current gain h_{FE} for each pair of values in the last table

Q2 *What range does h_{FE} lie in?*

SET

A	*B*	
1	6	1 - 10
2	1	10 - 20
3	5	20 - 40
4	3	100 - 400
5	4	500 - 1000
6	2	1000 - 2000

➲ *on-board SIS1*	**Turn switch S1 *ON***
➲ *SIS2*	**Press *INS***

Q3 *What has happened in the circuit and what is the reason for this?*

SET

A	*B*	
1	5	the power supply has been disconnected from the whole circuit and so nothing can be measured
2	3	the power supply has been disconnected from the collector and so I_C is zero
3	4	I_C is increased due to a transistor short-circuit between C and E
4	1	I_C is zero due to a disconnection of the base bias circuit
5	2	I_C is zero due to disconnection of the emitter

➲ **on-board *SIS1***	**Turn switch S1 to *OFF***

Relationship between Collector and Emitter currents

- vary the last circuit, disconnecting the ammeter from the transistor base; connect J5, disconnect J6, and connect the ammeter across 5 - 6 to measure the emitter current
- turn RV1 so that I_C=25mA, initially
- measure I_E for this value of I_C
- calculate the coefficient α

Q4 *What is the value of α ?*

SET

A	*B*	
1	2	always negative
2	5	more than 10
3	1	less than 10
4	6	a little over 1
5	4	a little under 1
6	3	always equal to 2

B13.3 SUMMARY QUESTIONS

Q5 *How many junctions are there in a NPN transistor?*

SET

A	*B*	
1	4	3
2	3	2
3	2	1
4	1	0

Q6 *Which ratio defines the amplification coefficient α of a transistor ?*

SET

A	*B*	
1	1	I_B/I_C
2	5	I_E/I_B
3	2	$(I_C - I_{CBO})/I_E$
4	4	I_C/I_E
5	3	$(I_C + I_{CBO})/I_E$

Q7 *Using the normal conventional direction for current flow, the correct equation for a BJT PNP is:*

SET

A	*B*	
1	4	$I_E = I_C + I_B$
2	1	$I_B = I_C + I_E$
3	2	$-I_E = I_B - I_C$
4	3	$I_E = I_B - I_C$

Q8 *The coefficients* α *and* β *are related by the equation :*

SET

A	*B*	
1	2	$\alpha/2 = \beta + 1$
2	4	$\alpha = (\beta - 1)/(\beta + 1)$
3	1	$\beta = \alpha/(1 - \alpha)$
4	3	$\beta = \alpha + 1$

Q9 *If* β= 50 *in a transistor, what is the value of* α *?*

SET

A	*B*	
1	5	0.96
2	6	0.98
3	2	1.02
4	1	0.90
5	3	0.5
6	4	1

Lesson B14: JFET and MOSFET FIELD-EFFECT TRANSISTORS

OBJECTIVES

- To find the output characteristic $I_D = f(V_{DS})$
- To find the transfer characteristic $I_D = f(V_{GS})$
- To use the FET as a :
  - small signal amplifier
  - DC current generator

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod.MU/EV), Individual control unit mod. SIS1/SIS2/SIS3 (optional).
- experiment module mod.MCM4/EV
- multimeter
- oscilloscope

B14.1 BASIC THEORY

The Junction Field Effect Transistor (JFET)

The field-effect transistor differs from the PNP or NPN bipolar transistors in its operation as well as in its structure. The current in the JFET (Junction Field Effect Transistor) consists of a single type of carrier. The JFET symbols, for N and P channels are shown in figure B14.1, while the physical models are outlined in figure B14.2. The terminal D is the Drain, G the Gate, S is the Source.

The main difference between a bipolar transistor and a FET is that a BJT controls one current (I collector) with another current (I base), while a FET controls a current (I Drain) with a voltage (V Gate-Source).

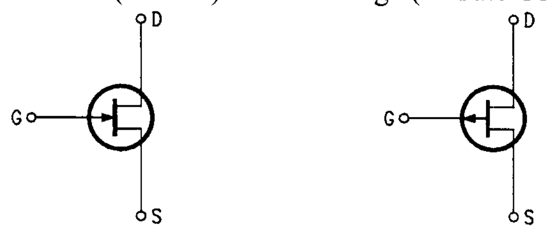


fig. B14.1

N channel *P channel*

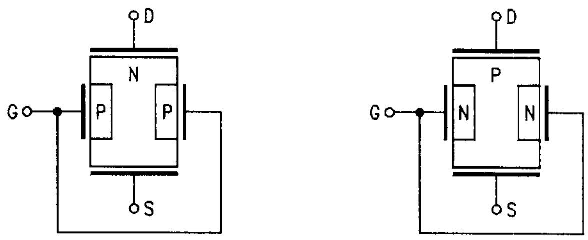


fig. B14.2

Operating principle

Consider an N channel JFET with dc voltages shown in figure B14.3.

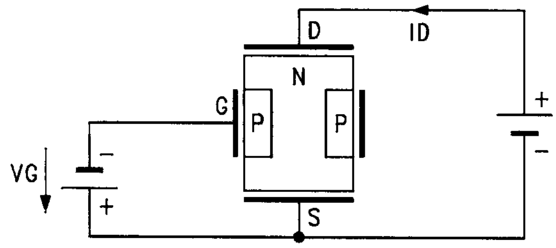


fig. B14.3

If the voltage V_G is zero, the current I_D flows through the resistance of the doped N type semi-conductor. If V_G increases, reverse biasing the PN junction, some of carriers in the junction region are removed. The volume of the region which has no carriers is proportional to this applied voltage (figure B14.4).

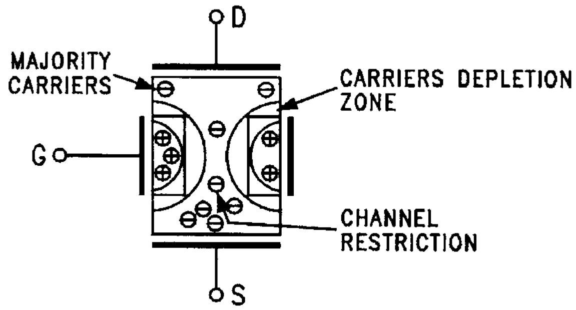


fig.B14.4

You can note that the N channel restricts, and that its conductivity decreases. In other words, the resistance between S and D increases as the volume of the depletion region increases. In normal operation the PN junction between Gate and Source is reverse biased. The input current is very low: this causes the the JFET to have a very high input impedance, of many Megaohm.

Suppose now we short-circuit the Gate and the Source and apply a voltage between them,$V_{DS} > 0$. As the Drain is at positive potential with respect to the Gate, the PN junction becomes more reverse biased the higher the voltage V_{DS} (figure B14.5). In these conditions a depletion region occurs which reduces the channel conductivity. Increasing the voltage V_{DS}, produces two opposed effects:

1. the current density between D and S increases
2. the channel resistance between D and S increases.

As the last effect is non linear with the voltage, a point is reached for a certain value of V_{DS} where the current I_D no longer increases. When $V_{GS} = 0$ Volt, the max. current between drain and source is called I_{DSS}. V_P (pinch-off voltage) is the minimum voltage V_{DS} for which the current I_D has a constant value I_{DSS}.

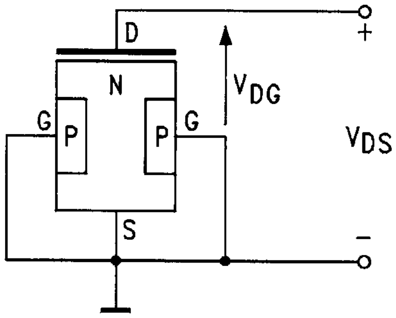


fig. B14.5

The current I_D is then proportional to the voltage V_{DS} and to the voltage V_{GS}. With $|V_{GS}| > V_P$, the channel is completely closed and $I_{DS} = 0$, irrespective of the voltage V_{DS}. This voltage value V_{GS} is called the disconnected voltage and is indicated by V_{GSoff}. Note that V_{GSoff} differs from V_P only in sign : $V_{GSoff} = -V_P$

Characteristic curves

The output, or Drain characteristics of an FET (fig.B14.6) show how the Drain current I_D depends on the Drain-Source voltage V_{DS} (for different values of the Gate-Source voltage V_{GS}). Note that:

- for $V_{DS}<V_P - |V_{GS}|$ the FET behaves as a resistor (ohmic region)
- for $V_{DS}>V_P - |V_{GS}|$ the current I_D does not depend on V_{DS} but depends only on V_{GS} (saturation region)
- when V_{GS} decreases (becomes more negative), so does I_D.

Mutual conductance characteristic

In the saturation region of the FET, I_D depends in practice only on V_{GS} (fig.B14.7). This dependence is expressed by the equation:

$$I_D = I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

where:

I_{DS} = Drain current in saturation region
I_{DSS} = Drain current for $V_{GS6} = 0$
V_P = Pinch-off voltage.

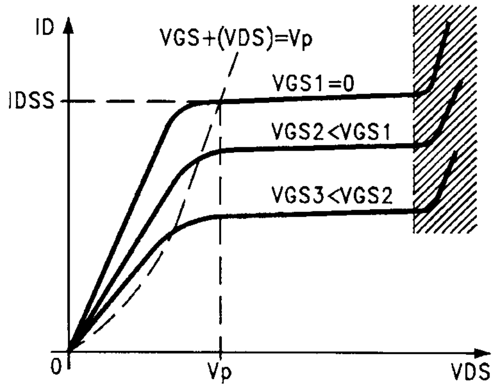


figure B14.6

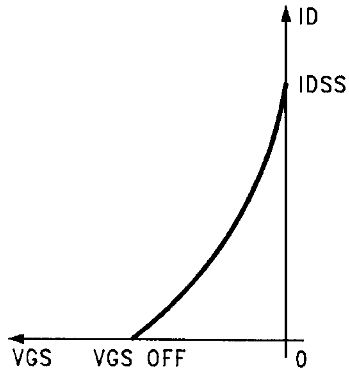


figure B14.7

The MOSFET

The "Metal-Oxide-Silicon FET" represents an evolution of the JFET in its technology and construction. Although its principle of operation is similar to the FET, it has a different structure. A thin layer of insulating oxide is placed between the Gate and the Drain-Source channel. For this reason, it is sometimes called an "Insulated Gate FET" (IGFET). There are two kinds of MOSFET. One type operates on the principle of carrier depletion, and the other on the principle of carrier enhancement. Their symbols are shown in figure B14.8.

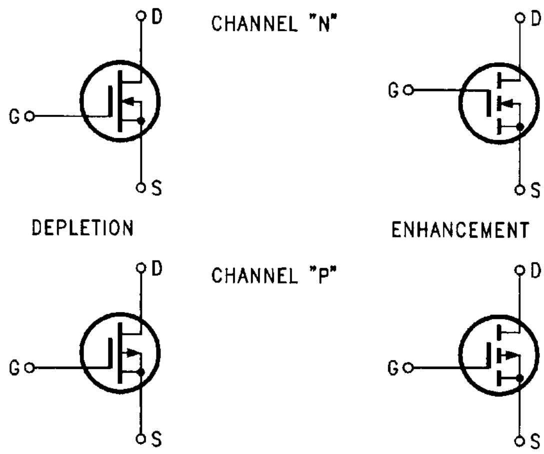


fig. B14.8

Depletion Type MOSFET

The structure of an N channel DEPLETION MOSFET is as shown in figure B14.9. As in the FET, the channel between D and S is continuous. It is supported by a lightly doped semiconductor base (P type), called the "Substrate". In the absence of Gate biasing, the MOSFET conducts with the carriers available in the channel. If the Gate is reverse biased, the channel is depleted of its carriers and conduction decreases. The

"Drain current" / "Drain-Source voltage" output characteristic is shown in figure B14.10.

This description of the N-channel MOSFET can also be applied to P-channel one, simply by reversing the direction of the currents and voltages.

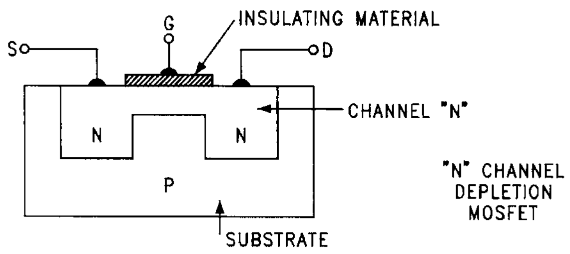


fig. B14.9

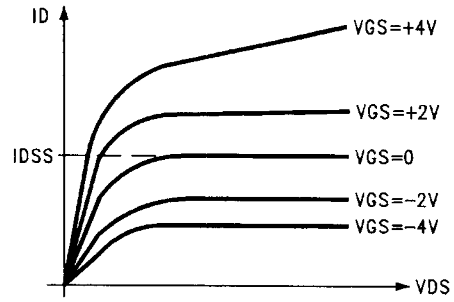


fig. B14.10

Enhancement Type MOSFET

The N channel Enhancement type MOSFET is shown in figure B14.11. It does not have a continuous channel between Drain and Source, and so it cannot conduct when there is no Gate biasing. However for $V_{GS} > 0$ negative carriers are attracted by the Gate into the area between S and D. An N-channel is created and the device can then conduct.

This is the only kind of FET which is cut off with $V_{GS} = 0$, and which controls the Drain current with a positive V_{GS}. This behavior is similar to a bipolar transistor. Figure B14.12. shows the "Drain current" / "Drain-Source voltage" output characteristic.

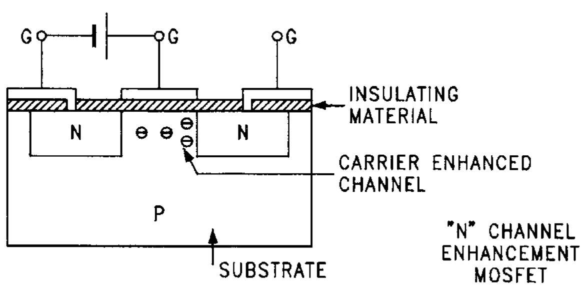


fig. B14.11

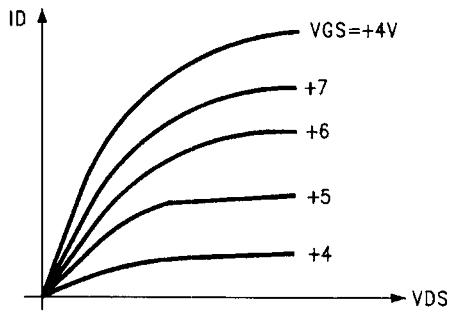


fig. B14.12

MOSFET compared to the JFET

The advantages of the MOSFET compared to the JFET are:

- as the Gate is insulated, these devices present an even higher input impedance than the JFET
- the Gate usually has a lower input capacitance, so the MOSFET shows a better response to high frequencies.

The disadvantage of MOS technology is that the insulating coating of SiO_2 can be damaged permanently by electrostatic discharges. They must be handled with care before connection to the circuit. One simple protection consists of short-circuiting the three pins. Another is to store them in anti-static material.

JFET Amplification circuit

The next lessons analyze in detail the different transistor amplifier configurations. In this lesson, we want to give you some general ideas on the subject by examining a JFET amplifier.

To use a FET as amplifier, chose a Gate biasing which gives operation in the linear region of the output characteristics. A variation of the voltage V_{GS} then produces a proportional variation in the current I_D:

$$I_D = g_m \cdot V_{GS}$$

where the parameter g_m is defined as the "transconductance" and gives the effect of the Gate voltage on the Drain current (fig.B14.13), in other words the gain.

Figure B14.14 shows a JFET amplifier circuit. Consider v_i and v_o as the input and output voltages. The voltage gain "Gv" of the amplifier, i.e. the ratio between the amplitudes of the output and input signals, is:

$$Gv = \frac{v_o}{v_i} \approx R_D \cdot g_m$$

The typical value of g_m is between 0.1 and 10 mA/V.

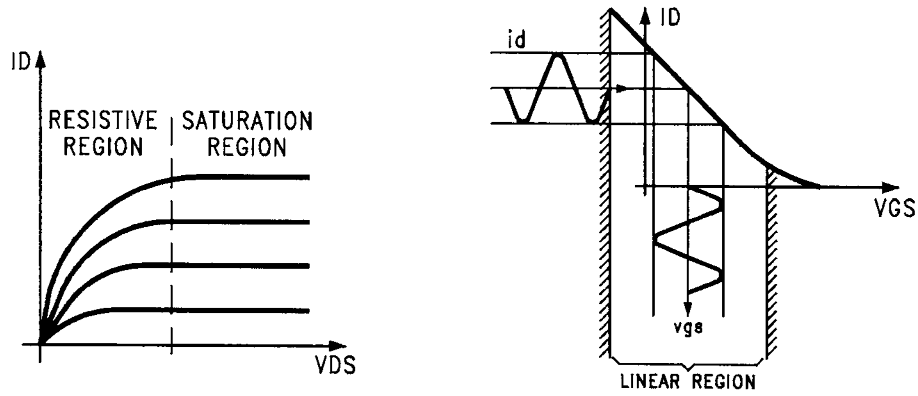


fig. B14.13

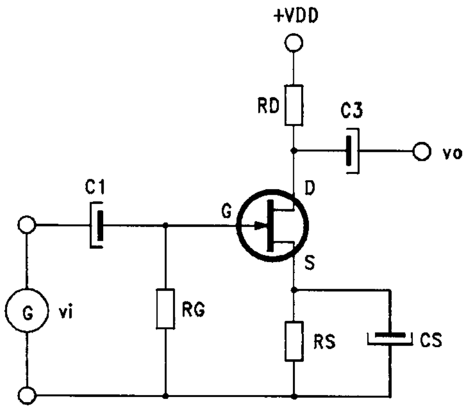


fig. B14.14

Constant current generator

Let's examine the JFET circuit.
An ideal current generator is a circuit which supplies a constant current, no matter what the load is. This source must have a very high output impedance. Figure B14.15 shows an example of a FET current generator.

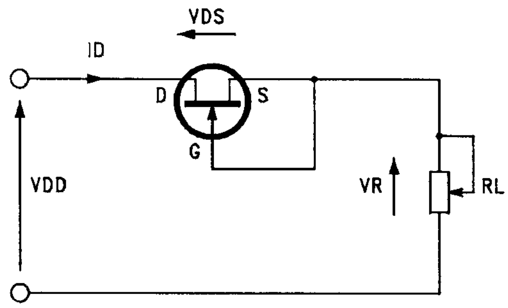


fig.B14.15

In this circuit, V_{GS} is equal to 0 Volt. If V_{DS} is greater than the voltage V_P, the current I_D in the circuit is constant and equal to I_{DSS}. The circuit is a constant current generator when V_{DS} exceeds V_P.

As $V_{DS} = V_{DD} - R_L \cdot I_D$, it follows that :

$$R_L < (V_{DD} - V_P) / I_{DSS}$$

If R_L is greater than this, the current rapidly decreases (figure B14.16).

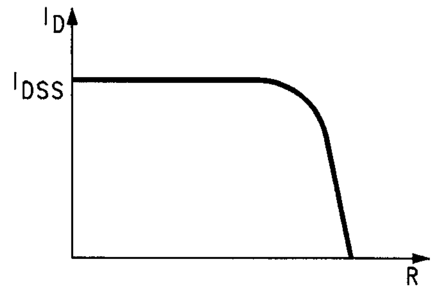


fig.B14.16

B14.2 EXERCISES

➲ *MCM4*	**Disconnect all jumpers**
➲ ***on-board SIS1***	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B14**

Determining the output characteristic of a JFET

- Connect jumpers J31, J32, J18, the ammeter between 23 and 24, the voltmeter (or the oscilloscope) between Drain and Source to produce the circuit of fig.B14.17

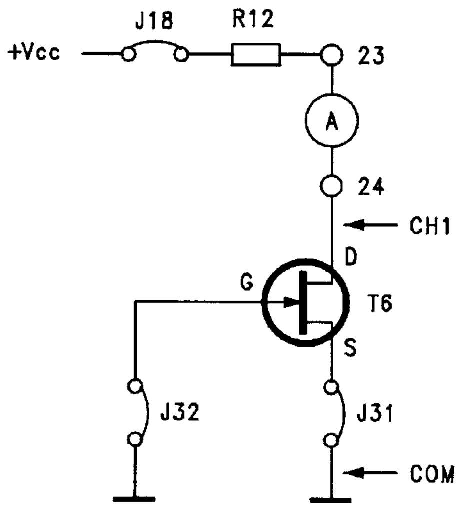
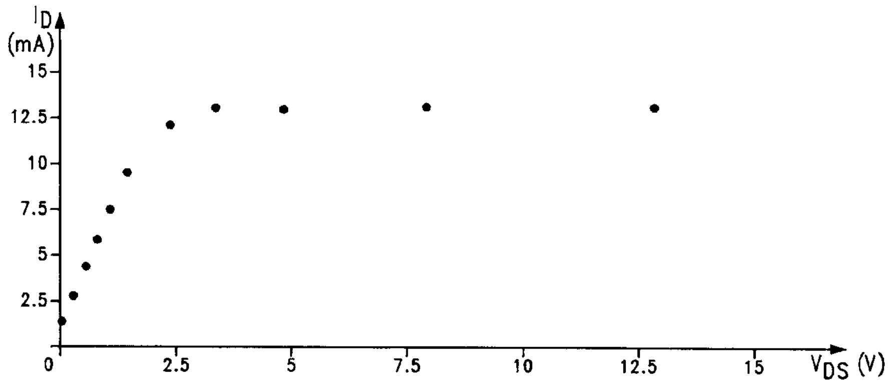


fig.B14.17

- Adjust the voltage Vcc of the variable power supply to 0 V initially. Then gradually increase Vcc and measure the current I_D into the circuit and the voltage V_{DS} of the FET for each value of Vcc in the following table:

V_{CC} (V)	1	2	3	4	5	6	8	10	12	15	20
V_{DS} (V)											
I_D (mA)											

- Plot the curve $I_D = f(V_{DS})$ (see next example) and find the pinch-off voltage V_P, and the saturation current I_{DSS}.



➲ ***on-board SIS1***	**Turn switch S4 *ON***
➲ ***SIS2***	**Press *INS***

Q1 *What has happened in the circuit?*

SET

A	*B*	
1	5	a resistor in series with R_{12} has been disconnected
2	3	the FET is short-circuited between the Drain and the Source
3	1	the FET is open-circuited between Drain and Source
4	2	the Gate circuit has been disconnected
5	4	the power supply voltage has decreased

➲ ***on-board SIS1***	**Turn switch S4 *OFF***

Determining the transfer characteristic

- Produce the circuit of fig.B14.18, by connecting jumpers J30, J37, J19, the ammeter and the voltmeter (or the oscilloscope) as shown in the figure

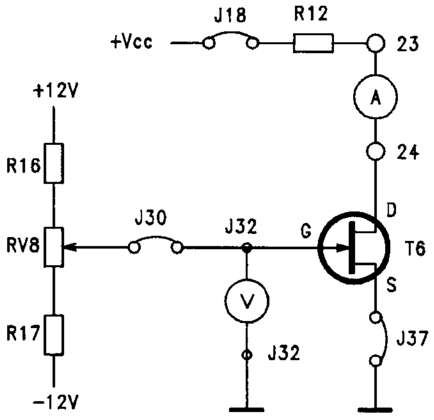
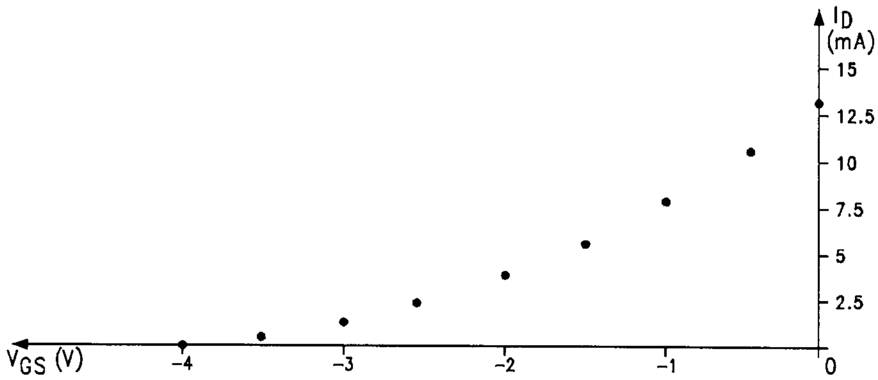


fig.B14.18

- vary V_{GS} by adjusting RV_8 and measure the current I_D for each value of the following table

V_{GS} [V]	0	-0.5	-1	-1.5	-2	-2.5	-3	-3.5	-4	-4.5
I_D [mA										

- evaluate the Gate voltage V_{Goff} for which the Drain current is reduced to zero
- plot the curve $I_D = f(V_{GS})$ (see next example), and evaluate the value of I_{DSS}



Q2 *How can the graph of* I_D *best be described?*

SET

A	*B*	
1	3	it has a max. at V_{GS} = -5 V
2	4	it is a straight line crossing the origin of the axes
3	5	it is a straight line parallel to the axis of V_{GS}
4	2	it is an arc of a circle whose center is the origin
5	1	it is a curve which decreases as V_{GS} decreases

Displaying the output characteristics on an oscilloscope

- Produce the circuit of fig.B14.19, by connecting jumpers J20, J21, J22, J33, J30
- set the oscilloscope to X-Y mode (50 mV/div on channel Y, 5V/div on channel X), and connect the probes as shown **(!!! use the differential probe for channel X !!!!)**. The voltage across R_{18} is proportional to the current I_D, and at the Drain the voltage is V_{DS}

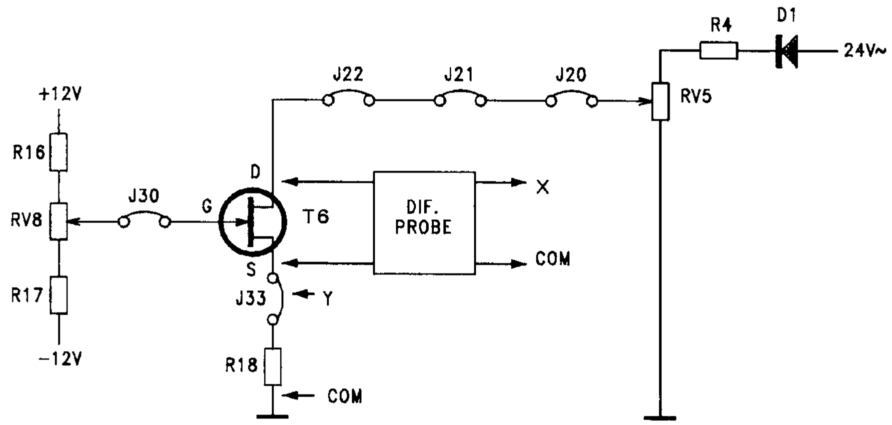


fig.B14.19

- vary V_{GS} by adjusting RV8, and check the variation of the curve $I_{DS} = f(V_{DS})$
- vary V_{DS} by adjusting RV5 and note how I_{DS} changes

Displaying the transfer characteristics on an oscilloscope

- produce the circuit of fig.B14.20 by connecting jumpers J19, J21, J22, J33, J25, J29, J26
- set the oscilloscope to X-Y mode (0.2 V/div on channel Y, 1V/div on channel X), and connect the probes as shown **(!!! use the differential probe for channel X !!!!)**. The voltage across R18 is proportional to the current I_D, and on the Gate the voltage is V_{GS}

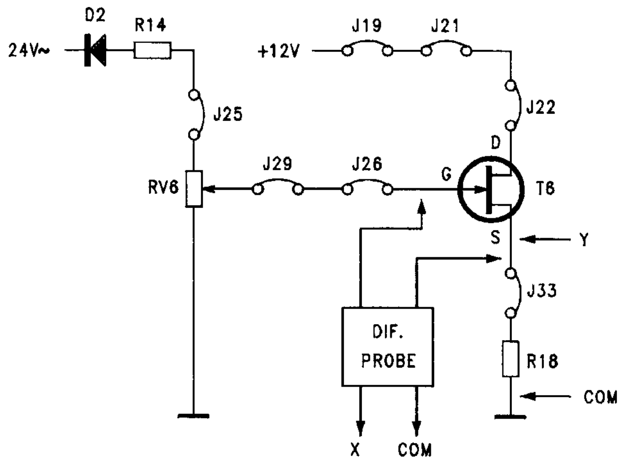


fig.B14.20

Q3 *From the display, note some characteristic points of the curve* I_D-V_{GS}. *For* $V_{GS}<V_P$ *what is* I_D ?

SET

A	*B*	
1	6	10 mA
2	5	12 mA
3	2	0 mA
4	3	5 mA
5	1	2 mA

- Calculate the slope of the curve for $-2V< V_{GS} < -0.5V$, which represents $g_m = \Delta I_D / \Delta V_{GS}$. You will find a value of g_m equal to some mA/V

Small signal (ac) amplifier circuit

- Adjust the variable power supply voltage Vcc to 24V.
- Connect jumpers J23, J24, J29, J27, J34, J36, J22, J18, to produce the circuit of figure B14.21
- connect the oscilloscope as shown in the figure, to display the input (v_i) and output signals (v_o) of the circuit
- use RV6 to adjust the input signal to 1 Vpp
- vary RV9 until you obtain the best possible sine wave on the output
- vary trimmer RV6, to increase the input voltage, and note the output signal distortion
- measure the peak-to-peak value of the output signal in absence of distortion
- calculate the amplification of the signal $G_V = v_o/v_i$

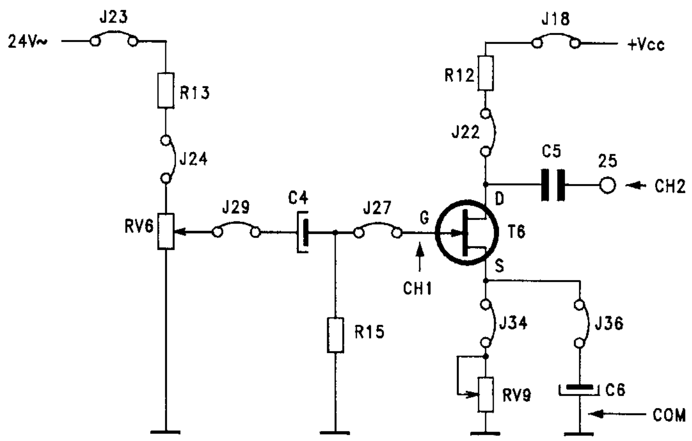


fig.B14.21

Q4 *What is the approximate amplification?*

SET		
A	*B*	
1	3	1
2	4	2
3	6	5
4	1	10
5	2	50

Constant current generator

- Adjust the variable power supply voltage to +24 Vdc. Connect jumpers J18, J21, J31, J34, the ammeter between points 23 and 24 and the oscilloscope as shown **(!!! use the differential probe !!!)**, to produce the circuit of figure B14.22

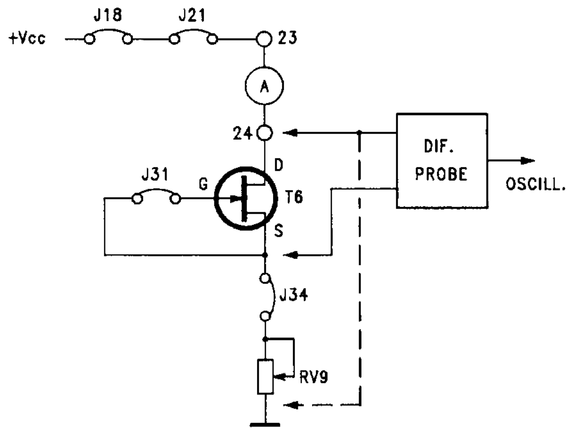


fig.B14.22

- minimize the resistance value of RV9 and measure the current into the circuit
- vary RV9 and note if the current remains constant. Note also the behaviour of the voltages V_{DS} and V_{RV9} (across the trimmer) on the oscilloscope

Q5 *How do the two voltages change as the resistance of RV_9 increases?*

SET		
A	*B*	
1	4	the two voltages stay the same
2	5	the two voltages decrease
3	2	the two voltages increase
4	1	the voltage V_{DS} increases, the other decreases
5	3	the voltage V_{DS} stays constant, the other increases

➲ ***on-board SIS1***	**Turn switch S8 *ON***
➲ ***SIS2***	**Press *INS***

Q6 *What happens to the circuit ?*

SET

A	*B*	
1	5	the FET is open
2	1	the FET is short-circuited
3	4	the power supply voltage has increased
4	2	missing power supply of T6 drain
5	3	none of the above

➲ ***on-board SIS1***	**Turn switch S8 *OFF***

B14.3 SUMMARY QUESTIONS

Q7 *What is a "channel" in a FET ?*

SET

A	*B*	
1	2	the region between gate and drain
2	5	the region between gate and source
3	4	the region between drain and source
4	3	the connection between the two gate regions
5	1	the input connection to the FET

Q8 *The drain-source channel is "cut-off" (and so* $I_D = 0$*) when:*

SET

A	*B*	
1	4	$V_{DS} = 0$ V
2	3	$V_{GS} = V_P$
3	1	$V_{GS} = 0$ V
4	5	$V_{GS} = -5$ V
5	2	$V_{DS} = -1$ V

Q9 *In its linear region a FET behaves as:*

SET

A	*B*	
1	2	a resistance
2	3	a diode
3	5	a capacitor
4	1	an inductor
5	4	an open switch

LESSON B15: OPTOELECTRONIC COMPONENTS

OBJECTIVES

- To study the resistance-luminosity characteristic of a photoresistor
- To study the current-luminosity characteristic of a photodiode
- To analyze the response of a photoresistor to light

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod. MU/EV), Individual Control Unit mod.SIS1/SIS2/SIS3 (optional).
- experiment module mod.MCM4/EV
- multimeter

B15.1 BASIC THEORY

The photoresistor

A photoresistor is a semiconductor device sensitive to electromagnetic radiation around the visible spectrum (wave-length between 380 and 760 nm). It has a very high resistance value in the dark, and its resistance drops when light radiation on it increases.

The photoresistor is made from a thin layer of semiconductor material, often cadmium sulfide (CdS). The incident light radiation gives part of its energy to the electron-hole pairs, which can reach an energy level sufficient to enter the conduction band. Consequently there are free carriers which increase conduction and so the resistance drops. The number of free carriers generated is approximately proportional to the intensity of the light radiation.

In practical applications an external voltage is connected across the photoresistor terminals. The carriers can then cross the device and flow in the external circuit.

Figure B15.1 shows the typical dependence of the resistance, R, of a photoresistor on the light intensity measured in lux.

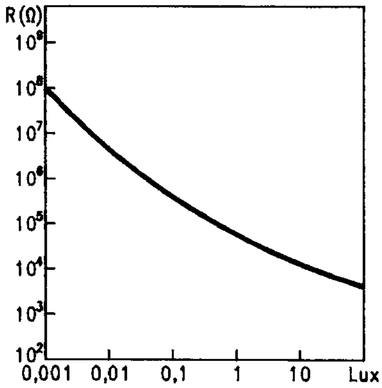


fig. B15.1

Photodiodes

A photodiode is similar to a normal semiconductor diode.
It is constructed so that light incident on the semi-conductor material is able to reach the junction region. The incident light energy on the electron-hole pair breaks their links, so the freed electrons are attracted back to the N type region, and the holes are attracted to the P type region.

A current (photocurrent) is thus generated by the diode, depending on the light intensity. The direction of this photocurrent is from the cathode to the anode; for this reason, in normal applications the photodiode is reverse biased.

When the photodiode is not illuminated, there is a weak dark current I_d across the junction, which is equal to the leakage current of a normal reverse biased diode.

When the device is illuminated, the total current I_t is the sum of the dark current I_d and the photocurrent I_p:

$I_t = I_d + I_p$

Figure B15.2 shows the voltage-current characteristics of a photodiode, at different values of incident light energy.

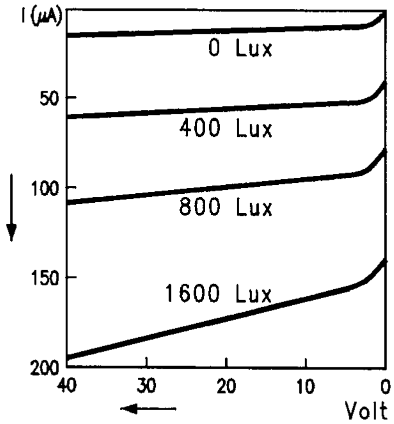


fig.B15.2

Phototransistors

A phototransistor is similar to a normal BJT transistor, with three layers of doped semiconductor materials, NPN or PNP.

The light radiation is concentrated onto the region near the collector-base junction. To understand the operation of an NPN phototransistor, suppose that the base-emitter junction is forward biased, while the collector-base is reverse biased. This is obtained applying a voltage V_{CE} with the collector at a higher potential than the base. With this biasing, the transistor operates in the active region.
Suppose that at start there is no incident radiation.

In this situation, there are only a few thermally generated carriers: the electrons cross the junction from the base to the collector, and the holes cross from the collector to the base. Together they constitute the reverse saturation current I_{cbo} of the collector junction.

The current is given by the equation

$$I_c = (1+ß)\cdot I_{cbo} + ß\cdot I_b$$

where I_b is the base current and ß the gain of the transistor.

Supposing the base is open circuit ($I_b = 0$), then this equation becomes:

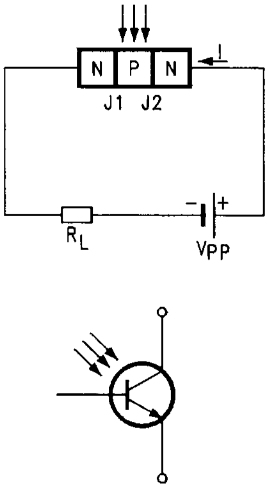
$$I_c = (1+ß)\cdot I_{cbo}$$

Now, if the device is illuminated, more minority carriers are generated by photoelectric effect. These contribute to the leakage current, in the same way as carriers generated by thermal effects. If I_p is the reverse leakage current component due to light, the total collector current is:

$$I_c = (1+ß)\cdot(I_{cbo} + I_p)$$

Note that the effect of the radiation on the transistor is to multiply the current produced by the factor (1+ß).

Figure B15.3 shows the "collector voltage-emitter current" curves of a N-P-N phototransistor for different values of the incident light intensity. If the base terminal is connected, and a base current I_b flows, the collector current is increased by the amount $ß\cdot I_b$.



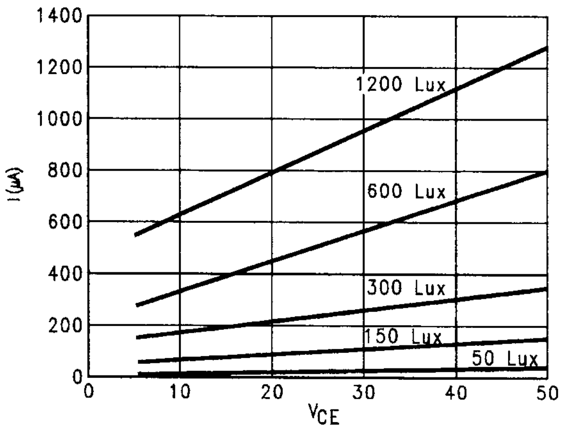


fig. B15.3

B15.2 EXERCISES

➲ *MCM4*	**Disconnect all jumpers**
➲ ***on-board SIS1***	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B15**

Resistance-light characteristic of the photoresistor

- Connect jumper J39, and connect the ohmmeter between points 30 and 31 to produce the circuit of figure B15.4.

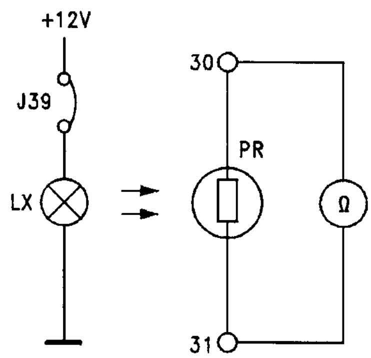


fig. B15.4

- photoresistors are made from semiconductor materials, so they are sensitive to temperature. To minimize the thermal effect of the lamp on the component, we suggest you carry out the measurement quickly, starting with the lamp at the closest distance to the photoresistor, and then progressively moving it away
- note the change in resistance as the light source is moved away

Q1 *What happens to the resistance?*

SET

A	*B*	
1	3	the resistance increases
2	4	the resistance stays constant
3	1	the resistance drops
4	5	the resistance stays constant at zero
5	2	the resistance stays constant, and is infinite

The light intensity striking the photoresistor is proportional to the power from the light source, and so to its distance. Clearly the closer the source, the higher is the intensity on the photoresistor. Qualitatively, the result is similar to that shown in figure B15.1.

Light-current characteristic of the photodiode

- Connect jumper J39 and the voltmeter across the resistance R20 (figure B15.5)

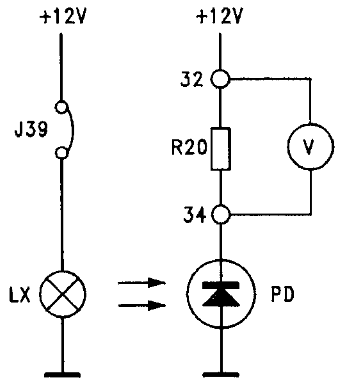


fig. B15.5

- When light falls on the surface of a photodiode, the diode behaves as a current generator, i.e. it "supplies" a reverse current proportional to the light intensity across it. The voltage across R_{20} is proportional to the current through it, and hence to photodiode illumination.
- move the lamp close to the photodiode and measure the voltage across R_{20}
- move the light source further away and repeat the measurements

Q2 *What happens to the measured voltage as the distance increases?*

SET

A	*B*	
1	4	the voltage increases
2	1	the voltage stays constant
3	2	the voltage drops
4	5	the voltage remains at zero
5	3	the voltage stays constant at 12 V

Phototransistor operation

- Connect jumper J39 and the voltmeter as in figure B15.6

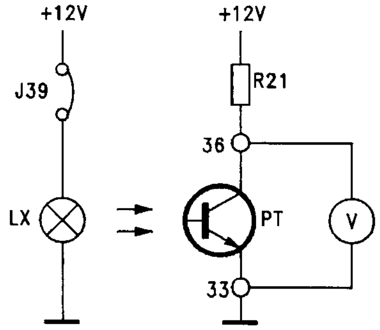


fig.B15.6

- measure the collector voltage with lamp off and check if the transistor conducts (with the lamp off, and with no light, the phototransistor should be cut off and so the voltage reading should be close to +12 V)
- turn on the lamp and place it close the phototransistor; measure the collector voltage

Q3 *What happens to the voltage when the light is on?*

SET

A	*B*	
1	5	the voltage stays constant
2	1	the voltage drops
3	4	the voltage increases
4	2	the voltage remains at zero
5	3	the voltage remains at 12 V

➲ ***on-board SIS1***	**Turn switch S9 *ON***
➲ ***SIS2***	**Press "INS"**

Q4 *In these conditions, is it possible to make the phototransistor conduct?*

SET

A	*B*	
1	4	no, because the power supply has been disconnected
2	3	no, because the base-emitter junction of the phototransistor is short-circuited
3	1	no, because the lamp does not have the necessary power
4	2	no, because there is a high resistance connected to the emitter

➲ ***on-board SIS1***	**Turn switch S9 *OFF***

B15.3 SUMMARY QUESTIONS

Q5 *A photoresistor is made from :*

SET

A	*B*	
1	3	a P-N junction
2	4	a layer of semiconductor material
3	2	a metal
4	5	an insulating material
5	1	a metal-semiconductor junction

Q6 *What part of the electromagnetic radiation spectrum is the photoresistor sensitive to?*

SET

A	*B*	
1	3	infrared
2	1	visible
3	4	ultraviolet
4	5	radio waves
5	2	gamma rays

Q7 *A photodiode consists of :*

SET

A	*B*	
1	4	a metal
2	1	a layer of semiconductor material
3	2	a P-N junction
4	5	a junction between two metals
5	3	none of the above

Q8 *In normal applications a photodiode :*

SET

A	*B*	
1	2	is not biased
2	1	is forward biased
3	4	is reverse biased
4	3	is biased with an a.c. voltage

Q9 *Where is the light radiation concentrated, in a phototransistor?*

SET

A	*B*	
1	3	onto the collector
2	1	onto the collector-base junction
3	5	onto the base
4	2	onto the base-emitter junction
5	4	onto the emitter

Q10 *In the dark the phototransistor collector current is:*

SET

A	*B*	
1	2	zero
2	4	determined by the leakage current of the C-B junction generated by thermal effects
3	1	determined by the leakage current of the B-E junction generated by thermal effects.
4	3	determined by the collector-emitter voltage

LESSON B16: TEMPERATURE TRANSDUCERS

OBJECTIVES

- To study the resistance-temperature characteristic of a thermistor

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod. MU/EV), Individual Control Unit mod.SIS1/SIS2/SIS3 (optional).
- experiment module mod.MCM4/EV
- multimeter

B16.1 BASIC THEORY

Thermistors are semiconductor devices whose resistance depends on temperature.

The thermoresistive effect in semiconductors is very different to the effect in metals.
In semiconductors, not only the mobility, but - more importantly - the number of carriers changes with temperature. At low temperatures electrons and holes do not have sufficient energy to pass from the valence band into the conduction band

Increasing the temperature however, gives the carriers enough energy to overcome the gap between the two bands, so the conductivity increases with temperature. In other words, when the temperature increases so does the conductivity, and consequently the resistance of the material drops.

Semiconductors have a NTC (negative temperature coefficient) of resistance. For an NTC material the law connecting the resistance to temperature is given by:

$$R_1/R_2 = e^{B\cdot(1/T1-1/T2)} \qquad B = W_b/K$$

where:

- R_1 and R_2 are the resistances at temperatures T_1 and T_2 respectively
- W_b is the energy of the band gap
- K is the Boltzmann constant.

Typical values for B range between 2000 °K and 5600 °K.
The first formula gives:

$$B = \frac{\ln(R_1/R_2)}{1/T_1 - 1/T_2}$$

Figure B16.1 shows a graph of the resistance dependence on temperature for NTC materials with different values of B.

Finally, note that thermosensitive devices can be produced with positive temperature coefficients, and so they are called PTC (positive temperature coefficient) materials.

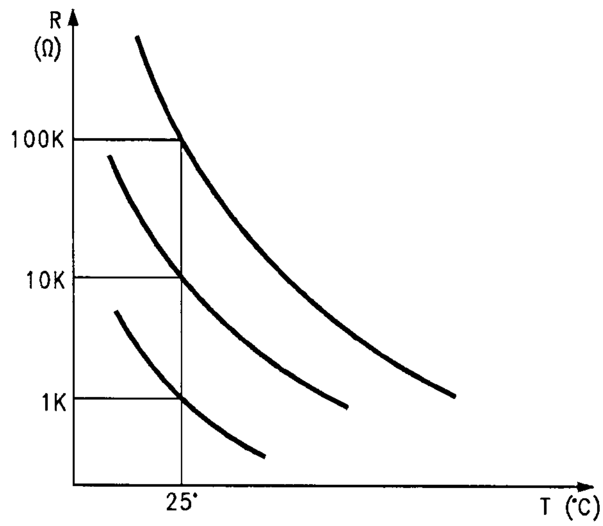


fig. B16.1

B16.2 EXERCISES

➲ *MCM4*	**Disconnect all jumpers**
➲ *on-board SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B16**

Resistance-temperature characteristic of a thermistor

- Produce the circuit in figure B16.2, connecting the ohmmeter between points 26-27

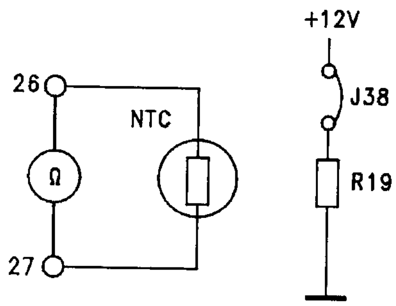


fig.B16.2

- Measure the resistance of the thermistor at ambient temperature
- Connect resistance to the power supply voltage by inserting jumper J38
- Note the behavior of the resistance as indicated by the meter, as R_{19} warms up

Q1 *How does the thermistor resistance change as the temperature increases?*

SET

A	*B*	
1	5	it stays constant
2	3	it drops
3	1	it drops by a small amount and then increases
4	2	it increases
5	6	it remains at zero
6	4	it becomes infinite

➲ *on-board SIS1*	**Turn switch S7 *ON***
➲ *SIS2*	**Press "INS"**

Q2 *What has happened to the circuit?*

SET

A	*B*	
1	4	resistance R_{19} has been cooled
2	5	the power to R_{19} has been disconnected
3	2	the thermistor has been disconnected
4	1	a resistance has been put in parallel with the thermistor
5	3	a low value resistance has been put in series with the thermistor

➲ *on-board SIS1*	**Turn switch S7** ***OFF***

- Disconnect J38 and wait for the resistance and thermistor to cool.
- Now connect the ohmmeter between points 28-29 to measure the resistance of a PTC thermistor at ambient temperature
- Connect J38 once more and observe the ohmmeter as the temperature rises

Unlike the previous case, you should find that the resistance of the PTC increases with temperature. However the temperature coefficient is positive only within a limited temperature range; outside it, the coefficient is negative. A typical behavior is shown in figure B16.3.

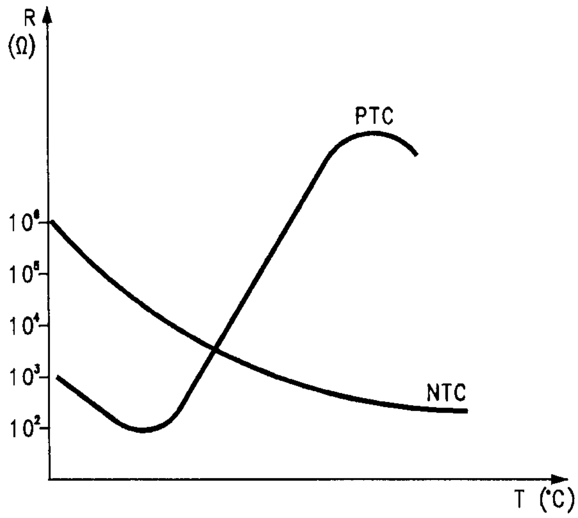


fig. B16.3

B16.3 SUMMARY QUESTIONS

Q3 *A thermistor is made from :*

SET

A	*B*	
1	2	a conductor
2	3	a semiconductor
3	5	a p-n junction
4	1	a junction of two metals
5	4	an insulating material

Q4 *The resistance-temperature characteristic of a NTC thermistor is:*

SET

A	*B*	
1	5	linear
2	4	quadratic
3	2	exponential
4	3	logarithmic
5	1	parabolic

Q5 *The resistance of an NTC thermistor:*

SET

A	*B*	
1	4	drops as the temperature increases
2	3	increases as the temperature increases
3	2	increases as the temperature increases up to 0°C, then drops
4	5	drops as the temperature increases up to 0°C and then increases
5	1	remains constant as the temperature is varied

Q6 *In a PTC device what happens to the resistance when the temperature increases?*

SET

A	*B*	
1	3	it increases
2	5	it drops
3	4	first it increases and then it drops
4	1	first it drops and then it increases
5	2	it remains constant

LESSON B17: AMPLIFIER CONFIGURATIONS

OBJECTIVES

- To analyze the different configurations (Common Base/ Emitter/Collector)
- To note the behavior of the characteristic curves
- To calculate the static current gain

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod. MU/EV), Individual Control Unit mod.SIS1/SIS2/SIS3 (optional)
- experiment module mod.MCM4/EV
- oscilloscope
- multimeter

B17.1 BASIC THEORY

A transistor amplifier can be connected in three different ways or configurations. These configurations are called the "common emitter", "common collector" or "common base", depending on which terminal is set to ground. That terminal is then the common reference for output and input.

Common Emitter Amplifier

As seen in fig. B17.1, the signal to be amplified is applied to the base terminal and the amplified output is taken from the collector.

If the applied voltage V_{BE} increases, the current I_B also increases, and so does the current I_C (as $I_C = h_{FE} \cdot I_B$).

This increase of I_C increases the voltage V_{RC} and, as $V_{RC} = V_{CC} - V_{CE}$, the output voltage V_{CE} decreases. Similarly when V_{BE} decreases, V_{CE} increases.

We see that:
- the amplifier is inverting, i.e. if the input voltage increases, the output voltage decreases and vice versa
- the voltage amplification rises as the value of R_C increases, as a variation in I_C produces a voltage variation which goes up as R_C increases.

A common emitter amplifier is the only one with a high current and voltage gain, and so the power amplification is very high (as $P=V \cdot I$).

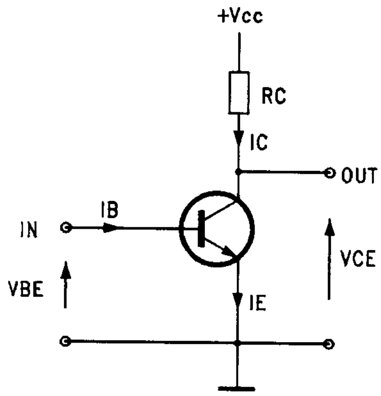


figure B17.1 Common Emitter amplifier

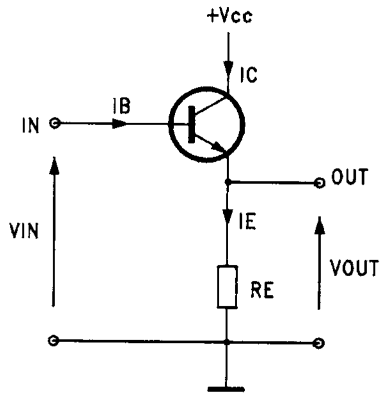


figure B17.2 Common Collector amplifier

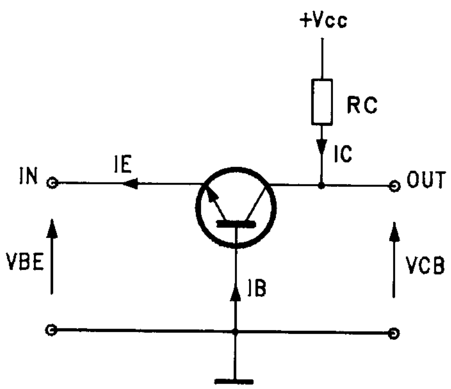


figure B17.3 Common Base amplifier

Common collector amplifier

In this configuration (fig.B17.2), the collector is the common terminal as it is the only one among the three which is linked to a fixed voltage (V_{CC}). However, for ease of reference, the input signal applied to the base and the output signal taken from the emitter are referred as usual, to the ground of the circuit (and not to the collector)

As V_{BE} is almost constant in a conducting transistor, any rise or fall of V_{IN} is transferred onto the emitter and so at the output we have:

$V_{OUT} = V_{IN} - V_{BE}$.

As a result :
- the amplifier is non inverting. If V_{IN} increases, V_{OUT} increases, too
- the voltage amplification is equal to 1, i.e. the emitter voltage variation is equal to the base variation. This configuration is also called an emitter follower, because the output follows the input.

The common collector amplifier does not at first seem to be of much use, as it does not amplify the input voltage. However it is widely used, because it has high input impedance and a low output impedance. Consequently it can handle input signals from a source of high impedance, and still deliver an ouput to a low impedance load. In other words, it is an impedance matcher.

Common Base Amplifier

In this configuration, whose general features are seen in fig. B17.3, the signal to be amplified is applied to the emitter and the amplified output is taken from the collector.

When the input voltage V_{EB} (which must always be negative) increases, this means that V_{BE} drops, the current I_B increases, too, and so does the current I_C. As $V_{CB} = V_{CC} - R_C \cdot I_C$, the output voltage increases.

Similarly, when V_{EB} drops, V_{CB} drops, too.

Note that:
- the amplifier is non inverting
- the voltage gain is proportional to the value of R_C
- the input circuit, as it is crossed by the emitter current I_E, has a very low impedance.

This configuration is particularly used in radio frequency circuits as the input impedance, in the order of tens of Ohm, matches the 50 Ohm characteristic impedance of antennas and transmission lines.

Summary table

The following table gives the expressions related to the characteristic parameters of the three typical amplifier configurations of transistors, where:

- R_S is the output resistance of the signal to be amplified (s = source)
- r_e is a parameter which is approx. $25mV/I_E$.

	Common emitter	Common collector	Common base
Input impedance R_{IN}	$\beta \cdot r_e$ - low	$\beta \cdot R_E$ - very high	r_e - very low
Output impedance R_{OUT}	R_C - high	$(R_S/\beta)//R_E$ - very low	R_C - high
Current gain (maximum) Ai	β - high	β - high	unity
Voltage gain Av	R_C / r_e - high	unity	R_C / r_e - high
Power gain A_P	Ai · Av - very high	Ai - high	Av - high
Phase relation between V_{IN} and V_{OUT}	180°	0°	0°

B17.2 EXERCISES

➲ ***MCM4***	**Disconnect all jumpers**
➲ ***on-board SIS1***	**Turn all switches *OFF***
➲ ***SIS2***	**Insert lesson code: B17**

Voltage and current measurements will be required on some circuits. If only a single multimeter is available, this will be used sometimes as a voltmeter or at other times as ammeter. When used as a voltmeter, remember to short-circuit the points of the circuit where the ammeter would be inserted.

Common emitter circuit

Curve $V_{BE} = f(I_B)$ with V_{CE} held constant

- Connect jumpers J1, J8, J6, the ammeter between 3-4 and the voltmeter (or the oscilloscope) between 4-8 to produce the circuit of fig.B17.4

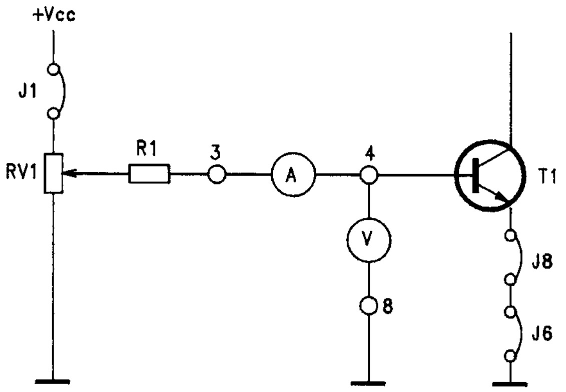
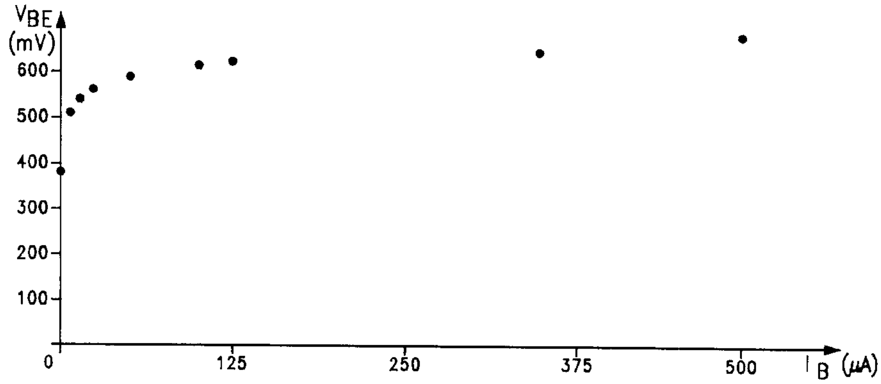


fig.B17.4

- measure the voltage V_{BE} for each value of the current I_B shown in the table:

I_B [µA]	0	5	10	20	40	80	100	300	500
V_{BE} [mV]									

- Plot the characteristic curve $V_{BE} = f(I_B)$ (I_B horizontal axis, see example in the next figure)



Q1 *The curve produced has a characteristic similar to a* :

SET

A	*B*	
1	3	resistance
2	4	UJT
3	2	diode
4	6	PTC
5	1	SCR
6	5	NTC

- calculate, at some point on the linear conduction region of the base-emitter junction, the static input resistance: $R_{IE} = V_{BE}/I_B$
- you should obtain a value of some thousands of Ohms for R_{IE}. A common emitter circuit has an average value for its static input resistance.

Curve $I_C = f(V_{CE})$ for constant I_B

- Connect jumpers J2, J6, J8, and the meters as indicated in fig.B17.5. The voltage V_{CE} can also be measured with an oscilloscope

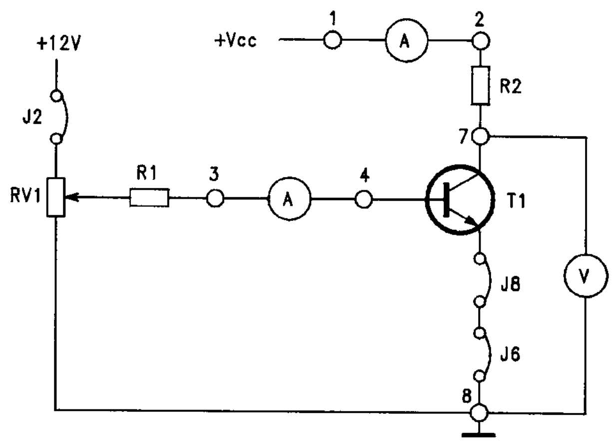


fig.B17.5

- adjust V_{CC} to 0V, and I_B to 20 μA
- increase the variable voltage V_{CC}. Measure the collector current I_C for the values of V_{CE} shown in the following table:

V_{CE} [V]	0.1	0.5	1	5	8	
I_C [mA]						I_B = 20 μA
						I_B = 40 μA
						I_B = 80 μA

- Plot a curve $I_C = f(V_{CE})$ for each value of I_B, and describe the behavior.

The collector current I_C increases rapidly with the voltage V_{CE} (when this is low), to become a linear,(almost horizontal), function of V_{CE} and proportional to the base current I_B. For small values of I_B, the curves are parallel in the linear region. For values of I_B over mA, the current I_C tends to take values proportional to the collector voltage V_{CE}. In the linear region the static output resistance is high.

- For V_{CE} = 5 V calculate, from the previous table, the static current gain $h_{FE} = I_C / I_B$ for each pair of values (I_C, I_B). Complete the following table with the data:

I_B [μA]	20	40	80
I_C [mA]			
h_{FE}			

The value found depends on I_C, and in particular it gradually increases with I_C to a certain value, dependent on the transistor, then finally it decreases.

➲ ***on-board SIS1***	**Turn switch S2 *ON***
➲ ***SIS2***	**Press "INS"**

Q2 *From measurements of the currents and voltages on the transistor we can say that:*

SET
A B

1 5 a higher resistance R_C has been inserted
2 3 the V_{CE} has been increased by changing V_{CC}
3 4 the base-emitter junction has been short-circuited
4 2 a resistance has been inserted in series with the emitter and the circuit is not a common emitter anymore
5 1 the emitter circuit is open-circuit and so I_C has been reduced to zero

➲ *on-board SIS1*	**Turn switch S2 *OFF***

Common base circuit

Curve $V_{EB} = f(I_E)$ with V_{CB} held constant

- Connect the instruments as shown in the diagram of fig.B17.6. The voltages can also be measured with the oscilloscope

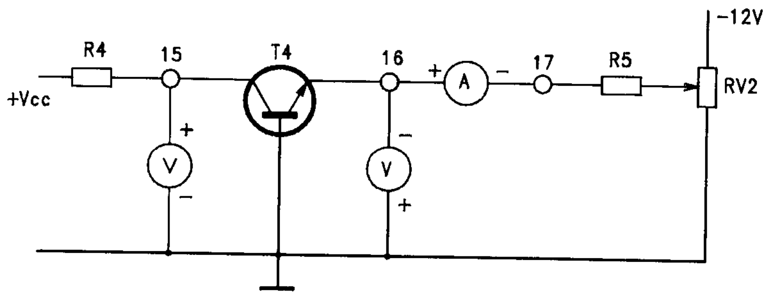


fig.B17.6

- keeping V_{CB} constant at 0.5 V, measure the emitter voltage V_{EB} for the values of IE given in the next table, and obtained by adjusting RV2

$V_{CB} = 0.5V$	I_E [mA]	0	0.05	0.1	0.3	0.5	1
	V_{BE} [mV]						

- plot the input characteristic $V_{EB} = f(I_E)$ for $V_{CB} = 0.5V$.

Q3 *What is the input resistance for this configuration, in the linear region ?*

SET

A	*B*	
1	2	it is very high
2	4	it depends on I_C and takes very different values
3	1	it is less than 1 KΩ
4	5	it remains at zero
5	3	it is infinite

Curve $I_C = f(V_{CB})$ for constant I_E

- Set Vcc to 0 V and I_E to 3 mA initially, by adjusting RV2
- Increase Vcc and calculate the collector current I_C , by measuring the voltage across resistance R4 (1Kohm), for each value of V_{CB} in the following table:

V_{CB} [V]	0	1	2	3	I_E (mA)
I_C (mA)					3
					1

- repeat these measurements for I_E = 1 mA
- draw the curve of I_C=f(V_{CB})
- compare the results of the output characteristics for the common base and common emitter connection
- calculate from the linear region of the curve I_C=f(V_{CB}) the static output resistance: $R_{OB} = V_{CB}/I_C$ on the characteristic at I_E = 3 mA.

Q4 *What is the calculated output resistance?*

SET

A	*B*	
1	5	it is zero
2	1	it lies between 10 and 100 Ω
3	2	approx. 100 KΩ
4	3	it lies between 1 KΩ and 10 KΩ
5	4	over 10 MΩ

Common collector circuit

Curve $V_{CB} = f(I_B)$ for constant V_{CE}

- Connect jumpers J1, J6, J7, J4, and the meters as in the circuit of figure B17.7. The voltages can also be measured with the oscilloscope

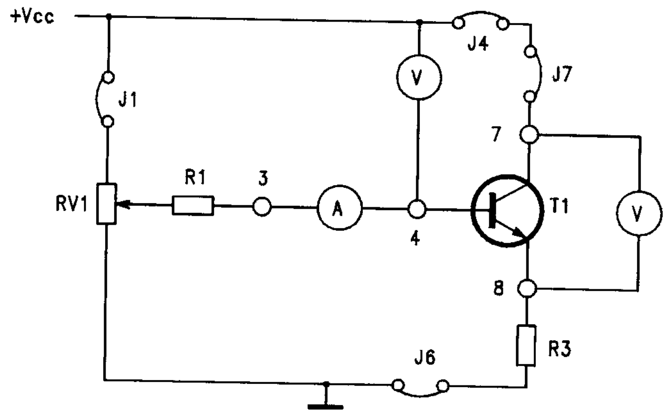
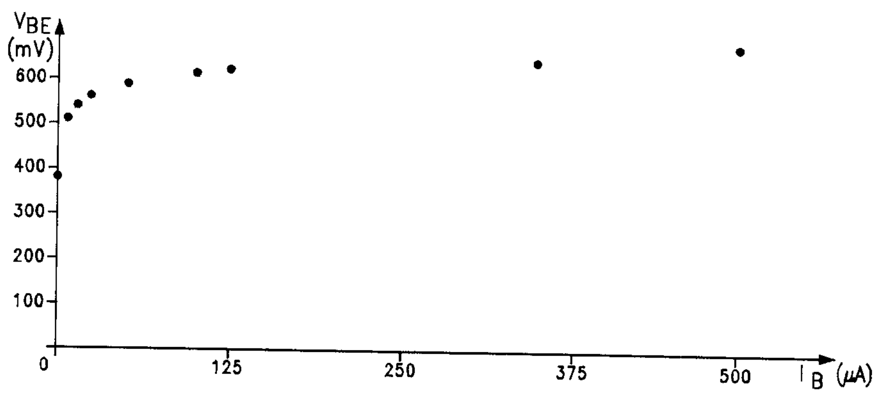


fig.B17.7

- adjust Vcc to obtain $V_{CE} = 5V$
- vary RV1 to obtain the current values I_B shown, keeping $V_{CE} = 5$ V constant. Measure the voltage V_{CB} for each value of I_B:

I_B [µA]	0	5	10	30	50	V_{CE} [V]
V_{CB} [V]						5
						10

- repeat these measurements for $V_{CE} = 10V$
- plot the characteristic input curves for each value of V_{CE} and describe their behavior



The curve $V_{CB} = f\,(I_B)$ depends on V_{BE}, and between B and E there is basically a diode. Once the base emitter junction is forward biased V_{BE} is constant at about 0.7V, so V_{CB} is constant, and equal to (V_{CE} - V_{BE})

- using the equation $R_{IC} = V_{CB} / I_B$ calculate the input resistance, R_{IC}

Q5 *What is the calculated input resistance of the common collector circuit ?*

SET

A	*B*	
1	3	zero
2	1	in the order of 100 Ω
3	4	in the order of 100 KΩ
4	5	around 1 MΩ
5	2	infinite

Curve $I_E = f(V_{EC})$ for constant I_B

The following measurements can only be made if two ammeters and a voltmeter are available.

- Connect jumpers J2, J7, J4, and the meters to produce the circuit of figure B17.8

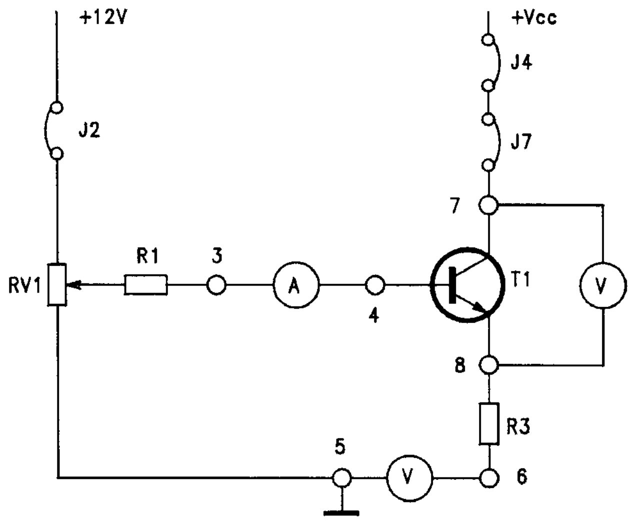


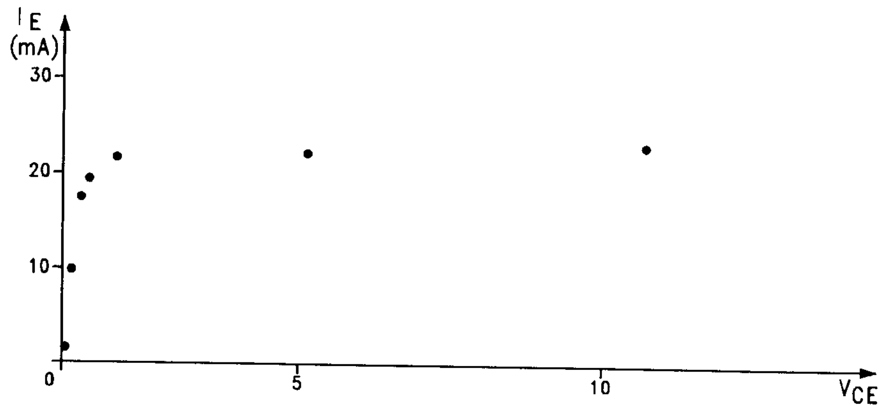
fig.B17.8

- adjust Vcc to 0V and I_B to 80μA. Gradually increasing Vcc, measure the emitter current I_E for each value of V_{CE} in the next table

V_{CE} [V]	0	0.1	0.3	0.5	1	5	10	I_B [μA]
I_E (mA)								80
								50

- Repeat the measurements for I_B = 50 μA

- Plot the characteristic output curve for each value of I_B



From the graphs you can note that, when the transistor starts conducting, I_E remains almost constant if V_{CE} is more than about 0.5V.

B17.3 SUMMARY QUESTIONS

Q6 *How many possible connections, or configurations are there for a transistor?*

SET

A	*B*	
1	4	1
2	1	2
3	6	3
4	5	4
5	2	5
6	3	6

Q7 *Which are the input parameters for an NPN transistor with common base connection?*

SET

A	*B*	
1	3	V_{BE}, I_B
2	1	V_{BC}, I_B
3	2	V_{EB}, I_E
4	5	V_{CE}, I_C
5	4	V_{EC}, I_B

Q8 *Which are the input parameters for a PNP transistor connected in a common collector configuration?*

SET		
A	*B*	
1	3	V_{BE}, I_B
2	1	V_{BC}, I_B
3	5	V_{EB}, I_E
4	2	V_{CE}, I_C
5	4	V_{CE}, I_B

Q9 *Which are the output parameters a NPN transistor in common collector connection:*

SET		
A	*B*	
1	2	V_{CB}, I_C
2	3	V_{EC}, I_E
3	5	V_{CE}, I_C
4	1	V_{CE}, I_B
5	4	V_{BE}, I_B

LESSON B18: TRANSISTOR BIASING

OBJECTIVES

- To determine the operating point and its position on the load line
- To understand class A, B and C biasing

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod. MU/EV), Individual Control Unit mod.SIS1/SIS2/SIS3 (optional)
- experiment module mod.MCM4/EV
- oscilloscope
- multimeter
- function generator

B18.1 BASIC THEORY

To bias a transistor means to fix the dc voltages and the currents so that they take a certain value, which corresponds a well defined point called the "Q", "quiescent" or "operating" point of the circuit.

The bias network consists of a number of components connected to the active device, to ensure its operation at the required point.

Biasing of a common emitter transistor

Circuit and output characteristic

A bias circuit for a common emitter amplifier is shown in figure B18.1. The external components are chosen so as to fix the variables I_C, V_{CE}, I_B to the required values. The three values, I_{CQ}-V_{CEQ}-I_{BQ}, define the "Q point" of the transistor.

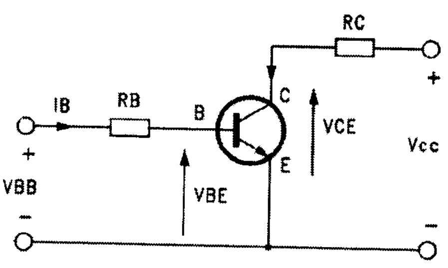


figure B18.1

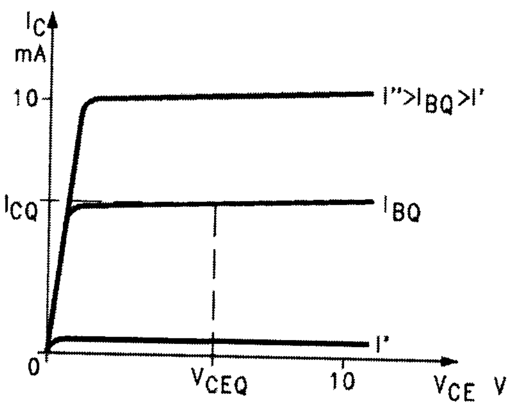


figure B18.2

Determining the bias components

To work out the component values needed to bias a transistor correctly, two methods can be used: a graphical one using the characteristic curves, or an analytical one.

Analytical method

1. Calculate the collector resistance R_C using the equation ($Vcc = V_{CE} + R_C \cdot I_C$). Rearranging this gives:

   $R_C = (Vcc - V_{CEQ})/I_{CQ}$ B18.1

   where Vcc is the power supply voltage

2. From the following equation, calculate the base current I_{BQ} which produces a collector current I_{CQ}:

   $I_{BQ} = I_{CQ} / \beta$ B18.2

   where β is the transistor current gain

3. Calculate the base resistance R_B using the equation $V_{BB} = V_{BE} + R_B \cdot I_B$:

   $R_B = (V_{BB} - 0.7) / I_{BQ}$ B18.3

   where 0.7V is the V_{BEQ} of the transistor, and V_{BB} is the dc voltage on the Base.

Graphical method

The "load line" of a bias circuit is defined as the line on the output characteristic of the transistor connecting the point (V_{CEM}, 0) to the point (0, I_{Csat}). V_{CEM} is the max. voltage between collector and emitter, and is equal to the power supply voltage Vcc, and I_{Csat} is the max. collector current, called "saturation current" ($I_C = I_{Csat}$ for $V_{CE} = 0$ Volt).

1. mark the "Q" point on the output characteristic

2. the value of I_{Csat} is determined, by drawing the load line to cut through the Q point and (V_{CEM} , 0) (figure B18.3)

3. the collector resistance R_C is calculated from the formula for the equation of the load line ($Vcc = V_{CE} + R_C \cdot I_C$):

   $R_C = Vcc / I_{Csat}$ B18.4

4. the value of I_{BQ} is found from the output characteristic, where the curve $I_C = f(V_{CE})$ crosses the Q point (I_{CQ} , V_{CEQ})

5. the value of V_{BEQ} which corresponds to I_{BQ} is determined from the input characteristic $V_{BE} = f(I_B)$

6. R_B is calculated using the equation relating the base and emitter voltages

$V_{BB} = V_{BE} + R_B \cdot I_B$, from which

$R_B = (V_{BB} - V_{BEQ}) / I_{BQ}$ B18.5

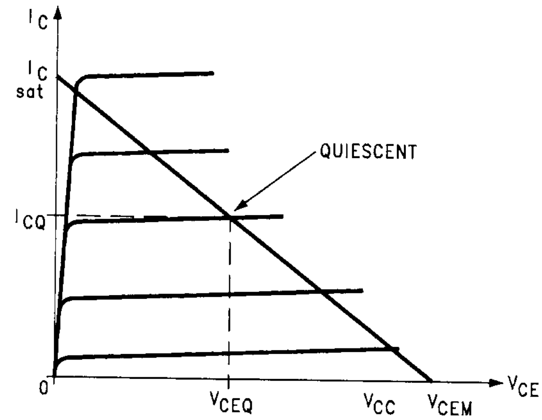


fig.B18.3

Operating regions of the transistor

In the output characteristic $I_C = f(V_{CE})$ we can define three different operating regions of the transistor (fig.B18.4):

- *region I*: V_{BE} is equal to 0 Volt and I_C takes very low values; V_{CE} depends only on the power supply voltage Vcc. In these operating conditions the transistor is "cut off " or "blocked"
- *region II*: I_C is a linear function of I_B and is practically independent of V_{CE}. In these conditions the transistor is in its "active" region
- *region III*: V_{CE} takes very low values and I_C depends only on the power supply voltage and the collector resistance R_C (I_{Csat} =Vcc / R_C). The transistor is fully on or in its "saturation" region.

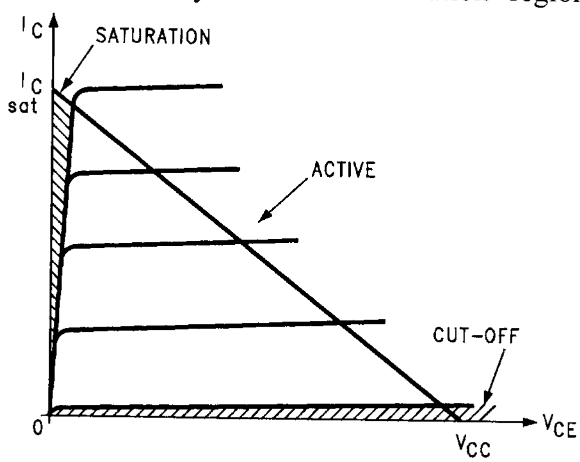


fig.B18.4

Bias circuit with a single power supply

The circuit of figure B18.1 can be obtained with a single power supply using a suitable potential divider (figure B18.5). The previous formulae for the determination of the Q point remain valid if the following substitutions are used:

$V_{BB} = Vcc \cdot R2 / (R2+R1)$ B18.6

$R_B = R1 \cdot R2 / (R1+R2)$ B18.7

$R1 = R_B \cdot Vcc / V_{BB}$ B18.8

$R2 = R_B \cdot Vcc / (Vcc - V_{BB})$ B18.9

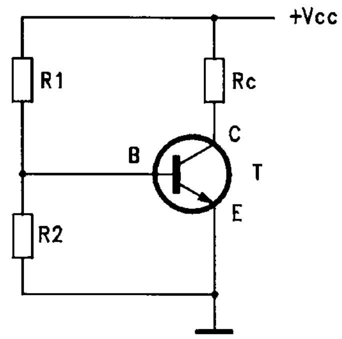


fig.B18.5

Classes of Operation

Transistor amplifier circuits can be classified using the general transfer characteristic as shown in figure B18.6.

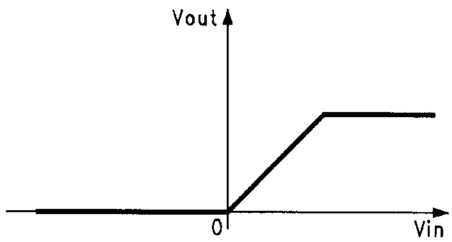


fig.B18.6

The signals to be amplified are normally time variable (ac). In some applications, only a part of the input wave is to be amplified; this is possible if a suitable point on the characteristic is chosen. The different operating modes can be put into three categories, called "class A", "class B" and "class C".

Class A

The operating point in the class A is located in the center of the straight section of the transfer curve. In this case, if base current excursions (caused by the input signal) stay within the linear region, the waveform across the output of the amplifier faithfully reproduces that of the input signal.

It follows that the collector current flows for the entire duration of the input signal cycle, and its average value is constant, and equal to that in the Q state. Figure B18.7 shows an example of amplification with a transistor biased for class A operation.

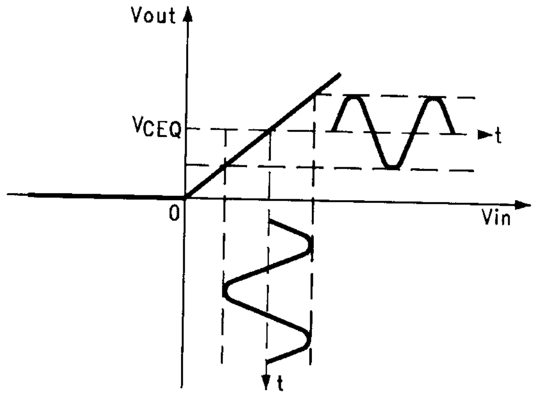


fig.B18.7

As the linear range over which the base and collector currents can vary is limited, it follows that it is not possible to "extract" all the power possible from the transistor. This max. power corresponds to the max. excursion possible of the collector current, i.e. from zero to saturation. The result is that the efficiency of the amplifier, defined as the ratio between the power supplied to the output (Po) and the power taken from the supply ($Vcc \cdot I_{CQ}$), is very low.

Class B

In this case, the Q point is placed close to the cut-off point of the transistor, so the collector current is very low (with no input signal). In the presence of a signal the current flows only during the positive part of the applied signal. The negative part of the input signal is less than the cut off value, and causes a complete cut-off of the collector current. Figure B18.8 shows this class B method of operation.

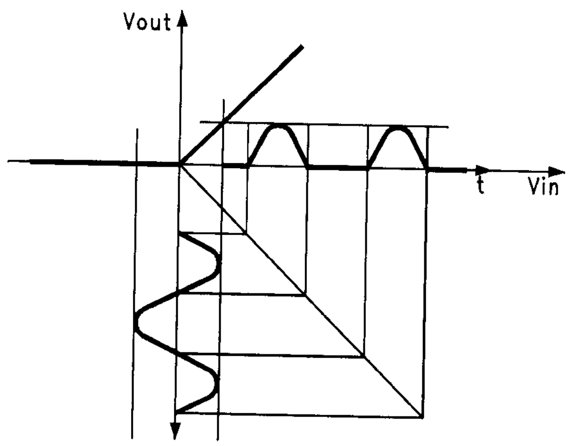


fig.B18.8

With an alternating signal, the collector current flows only for half a period, i.e. 180 degrees. This angle is called the conduction angle. To reconstruct the signal requires two transistors, conduct alternately: one for each half cycle. The typical efficiency of the class B operation is higher than class A.

Class C

In class C, the operating point is moved even lower than the cut-off point. The transistor supplies an output signal only if the input signal is at some point sufficiently large to exceed the cut off threshold. The conduction angle is further reduced compared to class B, being even less than 180 degrees. The collector current pulses are very narrow, with a duration less than half a period long. Figure B18.9 shows an example of class C amplification.

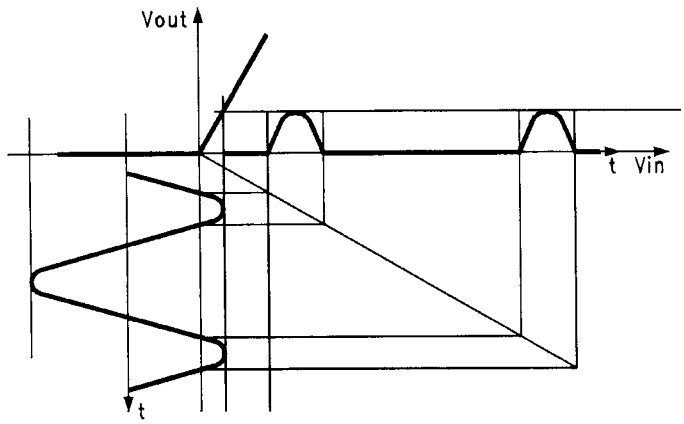


fig.B18.9

Although a class C amplifier produces a huge distortion in the output signal, it can operate with high efficiency.

B18.2 EXERCISES

➲ *MCM4*	**Disconnect all jumpers**
➲ *on-board SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B18**

Voltage and current measurements will be required on some circuits. If only a single multimeter is available, this will be used sometimes as a voltmeter or at other times as ammeter. When used as a voltmeter, remember to short-circuit the points of the circuit where the ammeter would be inserted.

Voltage and current measurements at the operating (Q) point

- Produce the circuit of fig.B18.10, connecting the jumpers J2, J6, J8 and the meters. The voltage measurement can be made with the oscilloscope

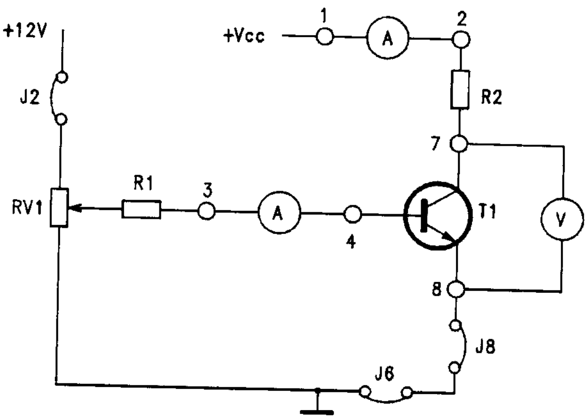


Fig.B18.10

- adjust Vcc to 20V, and using RV1, set I_B to 0
- increase I_B to obtain $I_C \approx 20$ mA and $V_{CE} \approx 10$ V

These settings bias the transistor at a Q point defined by:

- $I_{BQ} \approx 100\ \mu A$
- $I_{CQ} \approx 20$ mA
- $V_{CEQ} \approx 10$ V

- from the load line equation $Vcc = V_{CEQ} + R2 \cdot I_{CQ}$, calculate the saturation current I_{Csat}
- check this result practically by varying I_B with RV1. To determine the saturation current I_{Csat} ,try to make $I_B > 0.1$ mA.
- Determine the cut-off voltage V_{CEM} also, doing your best to make $I_B = 0$

Q1 *What is the voltage V_{CE} in saturation conditions (V_{CEsat}) ?*

SET

A	*B*	
1	4	10 V
2	5	7 V
3	6	2 V
4	2	5 V
5	3	1 V
6	1	0.2V

Class A amplifier

- Connect jumpers J10, J11, J14, J16, and the ammeter between points 20 and 21 as in figure B18.11.
- Adjust the function generator for a sine signal with amplitude 0 mV peak-to-peak and 1 KHz-frequency.

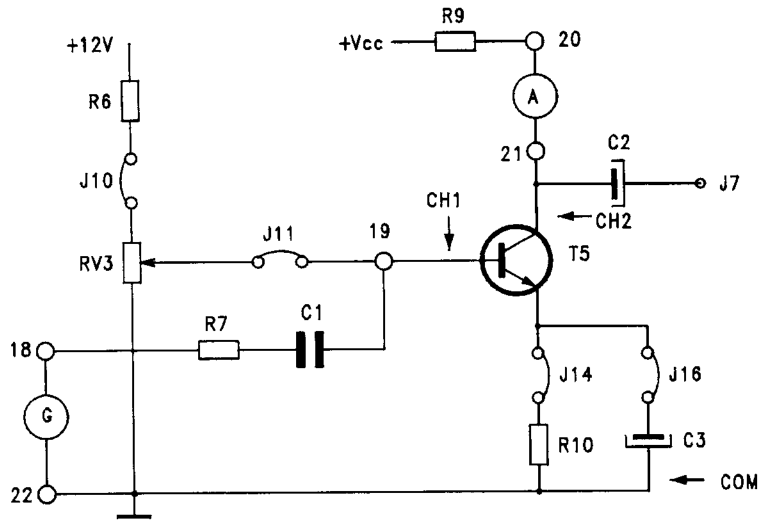


fig. B18.11

- set Vcc =20 V and adjust RV3 to obtain $I_{CQ} \approx 10$ mA

With no signal from generator G, the channel 2 of the oscilloscope displays a constant voltage equal to $V_{CEQ} + R10 \cdot I_{CQ}$

- progressively increase the amplitude of the signal supplied by the generator, until there is 50 mV peak-to-peak on channel 1 of the oscilloscope
- note the output voltage on channel 2

Q2 *What is the behavior of the output signal?*

SET

A	*B*	
1	3	the signal is a sine wave overlaid on a d.c. bias component
2	5	the signal is sine wave with zero average value
3	1	the signal is triangular wave
4	2	the signal is square-wave
5	4	the signal is sine wave with frequency double that of the input signal

Due to the signal applied to the Base of the transistor, we can say that the instantaneous Q point "moves" along the load line, producing a variable signal vce across the output. The excursions of the Q point on the load line are symmetrical with respect to the bias values V_{CEQ} and I_{CQ}.

- Move the channel 2 of the oscilloscope to the other side of capacitor C2, and display the output signal again

You will see that capacitor C2 enables us to decouple the output signal, that is to remove the dc component V_{CEQ}

- Increase the amplitude of the input signal, and note the behavior of the output signal on the oscilloscope

When the input voltage increases, the output signal has distortions, due to the fact that the excursions of the Q point then reach the saturation regions

Q3 *To obtain the max. signal without distortion at the output, what should* V_{CEQ} *be, in theory?*

SET

A	*B*	
1	6	$2 \cdot Vcc$
2	1	$Vcc - R9 \cdot I_{CO}$
3	4	Vcc
4	2	$Vcc/2$
5	3	$Vcc/4$
6	5	$R9 \cdot I_{CO}$

Amplifiers in class B and C

- In the circuit of fig.B18.11, adjust I_{CQ} to about 5 mA by means of RV3
- adjust the function generator for a sine wave signal with 50mV amplitude peak-to-peak and 1KHz frequency
- set channel 2 of the oscilloscope to DC
- slowly increase the bias voltage V_{CEQ} and reducing I_{BQ} , observing the behavior of the output voltage at the collector

Q4 *How does the displayed signal change?*

SET

A	*B*	
1	5	the signal becomes triangular
2	3	the signal is zero
3	4	the signal doubles its frequency
4	1	the signal becomes square-wave
5	2	the signal becomes distorted

This is because the transistor starts entering cut-off. If I_{BQ} continues to decrease, you will see a signal corresponding only to the positive half-waves of the input signal, which may raise the Q point above the cut-off region of the transistor.

The circuit now operates in class B, and so only the positive half waves of the input signal are amplified.

- reduce I_{BQ} again, and check the voltage across the transistor

For a low value of I_{BQ} the output signal can become zero, if the input signal does not have sufficient amplitude to take the transistor outside the cut-off region. If the circuit amplifies only a small part of the positive half wave (conduction angle < 180°), then the operation is in class C.

B18.3 SUMMARY QUESTIONS

Q5 *What does it mean to bias a transistor?*

SET

A	*B*	
1	4	to adjust the parameters I_B, Vcc and R_C to obtain the max. voltage and current gain
2	3	to adjust a circuit so that, at the operating point, the values of the output voltage and current are independent of the input ones
3	5	to adjust a circuit so that, at the operating point, the output and input voltages and currents take fixed values
4	1	to eliminate the dependence of the circuit's operation on temperature
5	2	to take the power supply voltage of the circuit to the optimum value

Q6 *The operation class of an amplifier depends on:*

SET

A	*B*	
1	3	the device used
2	4	the amplification value
3	5	the excursion of the signal which is needed
4	1	the power supply voltage
5	2	the biasing

Q7 *In a common emitter amplifier, the Q point (V_{CEQ} , I_{CQ}) and the power supply voltage* Vcc *are known. What is the collector resistance* R_C *?*

SET

A	*B*	
1	4	$(Vcc - V_{CEQ}) / I_{CQ}$
2	3	$(V_{BB} - V_{BEQ}) / I_{BQ}$
3	1	V_{CEQ} / I_{CQ}
4	5	$Vcc - V_{BB} / I_{BQ}$
5	2	$Vcc - V_{BB} / I_{CQ}$

Q8 *A single transistor amplifier produces an output signal which faithfully represents the input signal. What is its operating class?*

SET

A	*B*	
1	2	A
2	3	B
4	5	A-B
5	4	A-C

LESSON B19: Q POINT STABILIZATION

OBJECTIVES

- To study the self-heating effect of the collector current I_C and the effect of temperature on the base-emitter voltage V_{BE}
- To measure the gain variation in a common emitter amplifier with an emitter resistor
- To vary the output resistance of a circuit with collector-base resistance
- To stabilize the effect of the collector-base resistance

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod.PS1-PSU/EV or PSLC/EV, module holder structure mod. MU/EV), Individual Control Unit mod. SIS1/SIS2/SIS3 (optional).
- experiment module mod.MCM4/EV
- oscilloscope
- multimeter
- function generator

B19.1 BASIC THEORY

The Q point of a transistor can vary due to:
- temperature
- aging
- replacing the component (the characteristics of transistors, even of the same type have a large statistical spread).

Thermal effects

The collector current causes a power dissipation which results in an increase of the junction temperature.

The collector leakage current I_{CBO} is proportional to the junction temperature: we can say that it doubles for every 10° rise in temperature. As the collector current I_C is equal to $I_{CBO} + \alpha \cdot I_E$, the total collector current increases with the leakage current and so with the junction temperature.

Also the Base-Emitter voltage V_{BE} depends on temperature. When the temperature increases V_{BE} drops by about 2.5 mV/°C. It follows that I_B increases with temperature, and so I_C also increases.

Stabilization circuit with emitter resistor

One of the simplest ways to stabilize the operating point is to add a resistance R_E onto the emitter (figure B19.1).

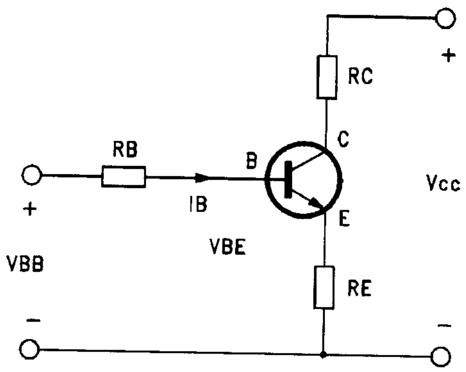


fig.B19.1

Suppose for example that I_{CQ} increases, then the voltage drop across R_E increases; it follows that the voltage V_{BEQ} falls, and with it the base current I_{BQ}, causing I_C to decrease. This is an example of negative feedback.

Stabilization circuit with collector-base resistance

The circuit of figure B19.2 also helps stabilize the Q point. If the collector current increases the voltage drop across R_C increases too, which reduces the collector voltage $V_{CE} = Vcc - I_C \cdot R_C$.. As I_B is approx. V_{CE} / R_F [actually $I_B = (V_{CE} - V_{BE})/R_F$], there is a reduction in the base current and so the collector current I_C tends to decrease.

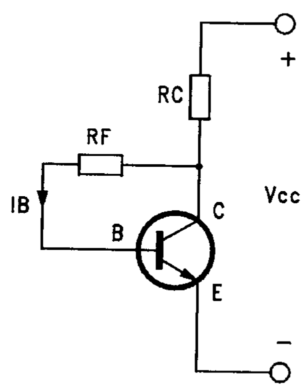


fig.B19.2

Circuit with emitter resistance: stability parameters

Influence of ICBO

Suppose for the moment that the only variable parameter is the reverse current of the base-collector junction (I_{CBO}): the current stability (Si) of the circuit is given by:

$$Si = \frac{\Delta I_C}{\Delta I_{CBO}} = \frac{\beta \cdot (R_B + R_E)}{(R_B + \beta \cdot R_E)} \qquad B19.1$$

or:

$$\frac{R_B}{R_E} = \frac{\beta \cdot (Si - 1)}{(\beta - Si)} \qquad B19.2$$

Note that the smaller Si is, the higher is the stability. A stability factor Si < 10 characterizes a good circuit – which in this case gives $R_B < 9 \cdot R_E$.

Influence of V_{BE}

Suppose now that the only variable is V_{BE}, with I_{CBO} and β constant. The stability voltage factor (Sv) is equal to:

$$Sv = \frac{\Delta I_C}{\Delta V_{BE}} = -\frac{1}{R_B/\beta + R_E} \qquad B19.3$$

You can say that a good circuit has a voltage stability less than 10%. In this case, with the $R_B < 9 \cdot R_E$ the formula becomes:

$$Sv = -1/R_E \qquad B19.4$$

This formula can be rearranged as :

$$\frac{\Delta I_C}{I_C} = -\frac{\Delta V_{BE}}{R_E \cdot I_C} \qquad B19.5$$

The stability is max. in this case for the max. value of $R_E \cdot I_C$. A variation of 5-10 % of I_C due to the variation of V_{BE} is usually acceptable. From equation B19.5, this will be the case if :

$$R_E \cdot I_C \approx 10\text{-}20 \cdot |V_{BE}| \qquad B19.6$$

Influence of the gain β

Suppose that the single variable is β with V_{BE} and I_{CBO} constant; the gain stability factor can be expressed as:

$$S_\beta = \frac{\Delta I_C}{\Delta \beta} = \frac{I_C \cdot S_{i2}}{\beta 1 \cdot (1+\beta 2)} \qquad \text{B19.7}$$

where S_{i2} is calculated with equation B19.1 for $\beta=\beta 2$. From this equation you can find R_B/R_E calculating S_{i2} , if $\beta 1$ and $\beta 2$ are known.

General guide

For a germanium transistor, a value of S in the order of 10 generally ensures a good stability for the current I_{CBO}. In this case the effects of variations in β are much reduced. In absence of data you can aim for a voltage drop across R_E equal to 1/10 of the power supply voltage (corresponding to R_E nine times less than R_B)

$$R_E \cdot I_C = Vcc/10 \qquad \text{B19.8}$$

$$R_B = 9 \cdot R_E \qquad \text{B19.9}$$

For a silicon transistor, the stability of the Q point essentially depends on the gain β, while the effect of I_{CBO} can be neglected. In absence of data, an emitter resistance can be chosen 30 times less than the base one:

$$R_B = 30 \cdot R_E \qquad \text{B19.10}$$

Effect of stabilization on the signal

The dynamic operation of an amplifier is altered by the stabilization network; in particular, the voltage amplification is considerably reduced. This effect can be overcome by making the stabilization network "invisible" for dynamic (ac) operation:

- in the circuit of fig. B19.3, the emitter is connected to ground (for the a.c. signal), by inserting a capacitor in parallel with R_E
- in the circuit of fig. B19.4, the mid point of R_F is set to ground by inserting a capacitor

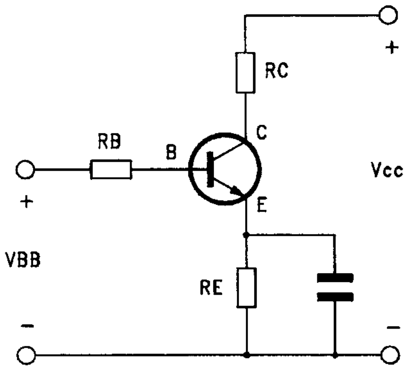


figure B19.3

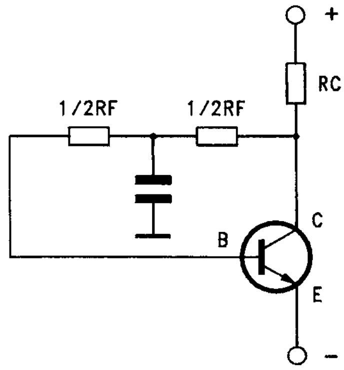


figure B19.4

B19.2 EXERCISES

➲ *MCM4*	**Disconnect all jumpers**
➲ *on-board SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B19**

Voltage and current measurements will be required on some circuits. If only a single multimeter is available, this will be used sometimes as a voltmeter or at other times as ammeter. When used as a voltmeter, remember to short-circuit the points of the circuit where the ammeter would be inserted.

Stabilization circuit with R_E

Observation of the effects of temperature

- Connect jumpers J10, J11, J15, and the meters as in figure B19.5, with Vcc set to 20 V
- Adjust trimmer RV3 make I_C about 10 mA
- connect jumper JT for a couple of minutes, to connect power to the heating resistor and heat up T5
- note how the voltage V_{BE} and current I_C change when the temperature increases. Lastly, disconnect jumper JT

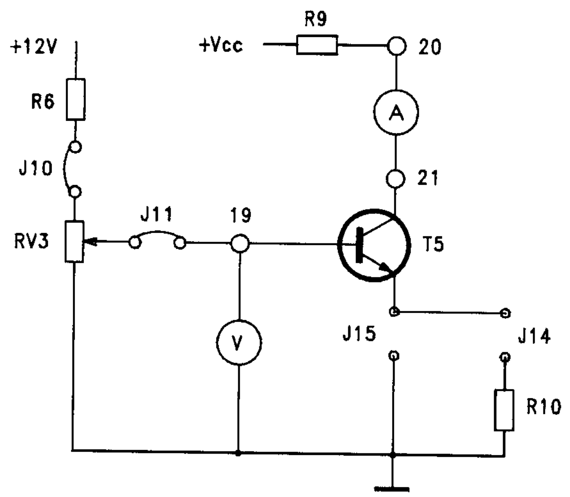


fig.B19.5

Q1 *When the temperature increases what happens to this voltage and current?*

SET

A	*B*	
1	3	the two variables are unaltered
2	5	the current drops and the voltage increases
3	1	the current stays constant and the voltage drops
4	2	the current increases and the voltage drops
5	4	the current goes to zero and the voltage increases

- Disconnect jumper J15 and connect the resistance R10 by inserting J14
- adjust trimmer RV3, to take the collector current to 10 mA
- connect JT again and repeat the last measurement

Due to the stabilization effect of $R_E = 100\ \Omega$ set in the emitter, you should find that the variation of V_{BE} and I_C are much smaller

- connect the ammeter across J11 and measure the base current I_B when the collector current is 10 mA
- calculate the static current gain $h_{FE} = I_C / I_B \approx \beta$

Q2 *What is the calculated current gain?*

SET

A	*B*	
1	5	$h_{FE} = 0 - 1$
2	3	$h_{FE} = 1 - 50$
3	4	$h_{FE} = 50 - 90$
4	2	$h_{FE} = 90 - 150$
5	1	$h_{FE} > 150$

- Disconnect jumpers J10, J11 and measure the resistance R_{BM} between the central terminal of the trimmer and ground
- calculate the equivalent base resistance R_B using B18.7:

$$R_B = \frac{R_{BM} \cdot [(RV3 - R_{BM}) + R6]}{RV3 + R6}$$

- with the values of ß and R_B determined above and using equation B19.3 calculate the stability factor Sv.

Q3 *What is the stability factor Sv ?*

SET

A	*B*	
1	6	between 1 and 2
2	5	between 2 and 3
3	4	between -1 and 0
4	1	between 20 and 30
5	3	between 10 and 20
6	2	between 0 and 1

Effect of R_E on the gain of an amplifier

- Connect jumpers J11, J15, J10 and the ammeter to produce the circuit shown in figure B19.6

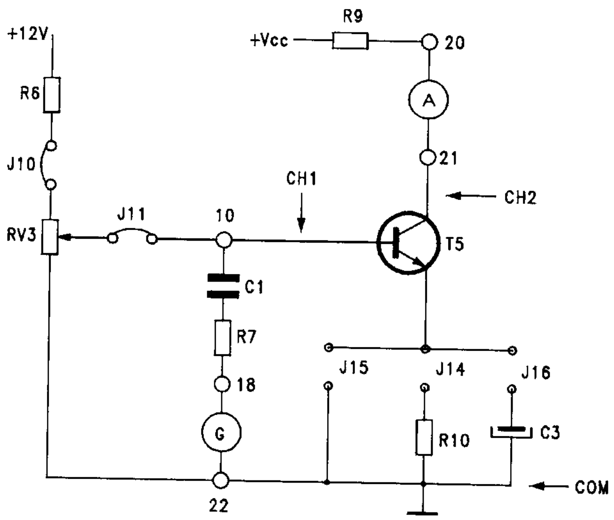


fig.B19.6

- set Vcc=20 V and adjust RV3 to obtain I_{CQ} = 10 mA
- adjust the function generator to a sine wave signal with amplitude of 50 mV peak-to-peak and 1KHz-frequency
- measure the peak-to peak voltage of the output signal on channel 2 of the oscilloscope, and calculate the voltage amplification Av of the circuit:

$$Av = Vout/Vin$$

The value of Av is about 300, although this value can vary, and depends on the h_{FE} of the transistor

- Disconnect jumper J15 and connect J14, to insert the resistor R10 into the emitter
- adjust RV3 to get I_{CQ} = 10 mA
- measure the output signal's voltage again and calculate the amplification for the modified circuit.

Q4 *The amplification has changed compared to the former circuit. Which has caused the change?*

SET

A	*B*	
1	3	the insertion of R_E which introduces a reaction in the circuit and increases the amplification
2	5	the insertion of R_E which increases the stability but reduces the amplification
3	1	an increase of the signal generator voltage
4	2	an increase of the transistor temperature
5	4	none of the above

Effect of the decoupling capacitor

- In the last circuit, connect jumper J16 to insert capacitor C3 in parallel with R10
- with the oscilloscope, measure the amplitude of the output signal, and calculate the voltage amplification
- compare this result with that obtained in the last chapter

The insertion of the decoupling capacitor C3 eliminates the feedback effect for the ac component of the signal. This gives a high gain (for ac) once more, similar to the gain that was obtained without R_E

➲ ***on-board SIS1***	**Turn switch S3 *ON***
➲ ***SIS2***	**Press "INS"**

Q5 *From measurements on the circuit, what fault has been inserted?*

SET

A	*B*	
1	4	the collector and the emitter of T5 are short-circuited
2	5	the circuit on the base of T5 is disconnected
3	1	the base and the emitter of T5 are short-circuited
4	3	the resistance R10 has been increased
5	2	the resistance R9 is disconnected

➲ ***on-board SIS1***	**Turn switch S3 *OFF***

Stabilization circuit with collector-base resistance

- Connect jumpers J12, J15 and the ammeter as in figure B19.7

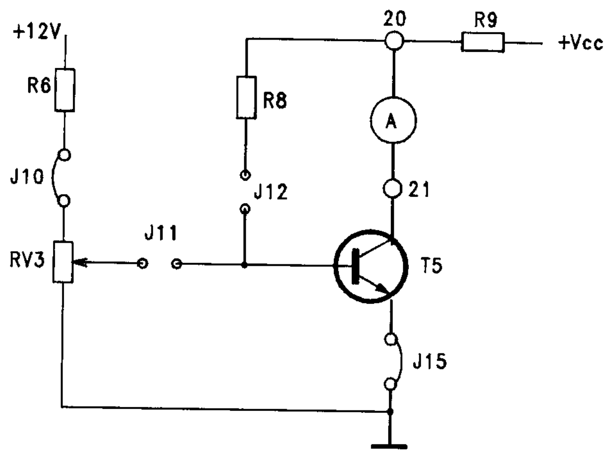


fig.B19.7

- Adjust voltage Vcc get a current I_{CQ} of 5 mA
- connect jumper JT for a few seconds, to provide power to the heating resistor and heat up transistor T5
- note the behavior of the current IC as the temperature increases. Then disconnect jumper JT and allow transistor T5 to cool
- disconnect jumper J12 and connect J10 and J11
- adjust trimmer RV3, and take the collector current to 5 mA
- insert JT again and repeat the last measurement

The variations of I_C are smaller when the feedback resistor R8 is inserted.

B19.3 SUMMARY QUESTIONS

Q6 *The purpose of the emitter resistance R_E is to:*

SET

A	*B*	
1	4	decrease the temperature of the collector-emitter junction
2	5	make the circuit less sensitive to temperature variations
3	1	calculate the emitter current
4	2	isolate the emitter from the circuit ground
5	3	protect the emitter from stray voltage pulses

Q7 *The stability of the operating point of a transistor is improved by inserting a :*

SET

A	*B*	
1	3	resistance between base and emitter and capacitance between emitter and ground
2	5	resistance between emitter and ground or capacitance between emitter and ground
3	2	resistance between collector and power supply
4	1	resistance between emitter and ground or resistance between collector and base
5	4	resistance between collector and base or capacitance between emitter and ground

Q8 *A circuit has a good stability when Si is:*

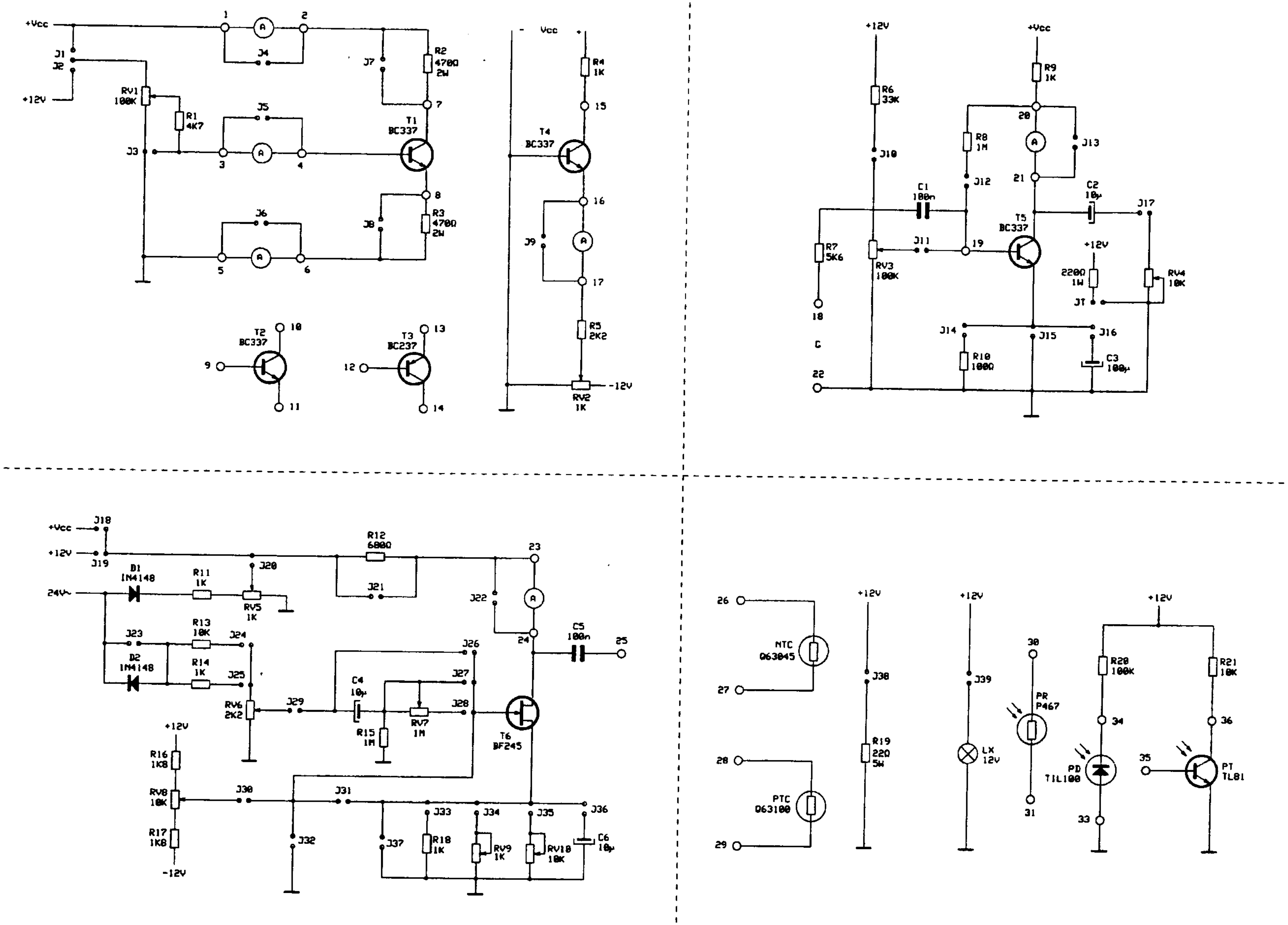
SET

A	*B*	
1	2	less than the 10%
2	4	more than the 10%
3	1	equal to the gain h_{FE}
4	5	$2 \cdot R_B/R_E$
5	3	calculated as operating point in the saturation region

Q9 *The operating point of a silicon transistor is stabilized with an emitter resistance R_E. What is a typical value for R_E ?*

SET

A	*B*	
1	3	$R_E=R_B/9$
2	5	$R_E=R_B/30$
3	4	$R_E=Vcc/(10 \cdot I_C)$
4	1	$I_C=10 \cdot I_B$
5	2	$Vcc=2 \cdot V_{CE}$



ELETTRONICA VENETA MOTTA DI LIVENZA - TV ITALY	DESCRIPTION : ELECTRONIC DEVICES AND CIRCUITS II	REPLACES: --	DWG Nº: MC841D01.FSH	DRAWN :
	EQUIPMENT : IPES MODULE MCM-4/EV	REPLACED BY: --	P.C.B.: MCM4	CHECKED :
	T.C. FILE : -- SCALE : --	REVISION: 0	SHEET : 1 OF 1	DATE : 09-01-97

APPENDIX "A": SYMBOLS USED

The following points sum up the notation used for the voltages and currents.

1. The instantaneous values of the variables varying in time are represented with small letters ("v" for the voltage and "i" for the current)

2. the average value of the variables in time, or quantities which remain constant, are represented by the corresponding capital letters ("V" for the voltage and "I" for the current)

3. the terminals of a device are identified by the first capital letter of the name of the terminal (B=Base; D=Drain, etc.)

4. the currents in a device have an index letter corresponding to the terminal to which they refer to (e.g.: i_B, I_B, i_b, Base currents; i_D, I_D, i_d, Drain currents). The voltages between two terminals are identified by the indexes indicating those terminals (e.g.: v_{be}, v_{BE}, V_{BE}, - voltage between Base and Emitter)

5. the maximum value and the average value have the index in capitals (e.g.: i_B, I_B for the currents; v_{BE}, V_{BE} for the voltages)

6. the index for ac, or incremental components is in small letters (e.g.: i_b for the currents; v_{be} for the voltages).

7. the power supply voltage is usually indicated by repeating the capital index of the electrode to which it refers to, e.g. V_{CC} (although this symbol is sometimes used indiscriminately when the power is applied to other terminals, such as the Drain or Anode)

APPENDIX "B": DATA SHEETS

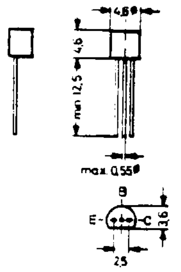
- transistor NPN BC337
- transistor PNP BC327
- JFET BF245
- phototransistor TIL81
- photodiode TIL100
- photoresistor NSL467
- RTD PTC thermistor
- RTD NTC thermistor

BC337, BC338

NPN Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups -16, -25 and -40, according to their DC current gain. As complementary types the PNP transistors BC327 and BC328 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC337** **BC338**	V_{CES} V_{CES}	50 30	V V
Collector Emitter Voltage	**BC337** **BC338**	V_{CEO} V_{CEO}	45 25	V V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	800	mA
Peak Collector Current		I_{CM}	1	A
Base Current		I_B	100	mA
Power Dissipation at $T_{amb} = 25\ °C$		P_{tot}	625[1]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 to +150	°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC337, BC338

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at V_{CE} = 1 V, I_C = 100 mA **BC337, BC338**	h_{FE}	100	–	630	–
Current Gain Group 16	h_{FE}	100	160	250	–
25	h_{FE}	160	250	400	–
40	h_{FE}	250	400	630	–
at V_{CE} = 1 V, I_C = 300 mA **BC337, BC338**	h_{FE}	60	–	–	–
Current Gain Group 16	h_{FE}	60	130	–	–
25	h_{FE}	100	200	–	–
40	h_{FE}	170	320	–	–
Collector Cutoff Current					
at V_{CE} = 25 V **BC338**	I_{CES}	–	2	100	nA
at V_{CE} = 45 V **BC337**	I_{CES}	–	2	100	nA
at V_{CE} = 25 V, T_{amb} = 125 °C **BC338**	I_{CES}	–	–	10	µA
at V_{CE} = 45 V, T_{amb} = 125 °C **BC337**	I_{CES}	–	–	10	µA
Collector Emitter Breakdown Voltage					
at I_C = 10 mA **BC338**	$V_{(BR)CEO}$	20	–	–	V
BC337	$V_{(BR)CEO}$	45	–	–	V
Collector Emitter Breakdown Voltage					
at I_C = 0.1 mA **BC338**	$V_{(BR)CES}$	30	–	–	V
BC337	$V_{(BR)CES}$	50	–	–	V
Emitter Base Breakdown Voltage at I_E = 0.1 mA	$V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at I_C = 500 mA, I_B = 50 mA	V_{CEsat}	–	–	0.7	V
Base Emitter Voltage at V_{CE} = 1 V, I_C = 300 mA	V_{BE}	–	–	1.2	V
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1)]	K/W

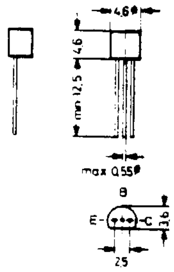
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC327, BC328

PNP Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups −16, −25 and −40, according to their DC current gain. As complementary types the NPN transistors BC337 and BC338 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC327** **BC328**	$-V_{CES}$ $-V_{CES}$	50 30	V V
Collector Emitter Voltage	**BC327** **BC328**	$-V_{CEO}$ $-V_{CEO}$	45 25	V V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	800	mA
Peak Collector Current		$-I_{CM}$	1	A
Base Current		$-I_B$	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 ... +150	°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC327, BC328

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA **BC327, BC328**	h_{FE}	100	–	630	–
Current Gain Group 16	h_{FE}	100	160	250	–
25	h_{FE}	160	250	400	–
40	h_{FE}	250	400	630	–
at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA **BC327, BC328**	h_{FE}	60	–	–	–
Current Gain Group 16	h_{FE}	60	130	–	–
25	h_{FE}	100	200	–	–
40	h_{FE}	170	320	–	–
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1]	K/W
Collector Cutoff Current					
at $-V_{CE}$ = 25 V **BC328**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 45 V **BC327**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 25 V, T_{amb} = 125 °C **BC328**	$-I_{CES}$	–	–	10	μA
at $-V_{CE}$ = 45 V, T_{amb} = 125 °C **BC327**	$-I_{CES}$	–	–	10	μA
Collector Emitter Breakdown Voltage					
at $-I_C$ = 10 mA **BC327**	$-V_{(BR)CEO}$	45	–	–	V
BC328	$-V_{(BR)CEO}$	25	–	–	V
Collector Emitter Breakdown Voltage					
at $-I_C$ = 0.1 mA **BC327**	$-V_{(BR)CES}$	50	–	–	V
BC328	$-V_{(BR)CES}$	30	–	–	V
Emitter Base Breakdown Voltage at $-I_E$ = 0.1 mA	$-V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at $-I_C$ = 500mA, $-I_B$ = 50 mA	$-V_{CEsat}$	–	–	0.7	V
Base Emitter Voltage at $-V_{CE}$ = 1V, $-I_C$ = 300 mA	$-V_{BE}$	–	–	1.2	V
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA **BC327, BC328**	h_{FE}	100	–	630	–
Current Gain Group 16	h_{FE}	100	160	250	–
25	h_{FE}	160	250	400	–
40	h_{FE}	250	400	630	–
at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA **BC327, BC328**	h_{FE}	60	–	–	–
Current Gain Group 16	h_{FE}	60	130	–	–
25	h_{FE}	100	200	–	–
40	h_{FE}	170	320	–	–
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1]	K/W
Collector Cutoff Current					
at $-V_{CE}$ = 25 V **BC328**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 45 V **BC327**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 25 V, T_{amb} =125 °C **BC328**	$-I_{CES}$	–	–	10	µA
at $-V_{CE}$ = 45 V, T_{amb} =125 °C **BC327**	$-I_{CES}$	–	–	10	µA
Collector Emitter Breakdown Voltage					
at $-I_C$ = 10 mA **BC327**	$-V_{(BR)CEO}$	45	–	–	V
BC328	$-V_{(BR)CEO}$	25	–	–	V
Collector Emitter Breakdown Voltage					
at $-I_C$ = 0.1 mA **BC327**	$-V_{(BR)CES}$	50	–	–	V
BC328	$-V_{(BR)CES}$	30	–	–	V
Emitter Base Breakdown Voltage at $-I_E$ = 0.1 mA	$-V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at $-I_C$ = 500mA, $-I_B$ = 50 mA	$-V_{CEsat}$	–	–	0.7	V
Base Emitter Voltage at $-V_{CE}$ = 1V, $-I_C$ = 300 mA	$-V_{BE}$	–	–	1.2	V
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

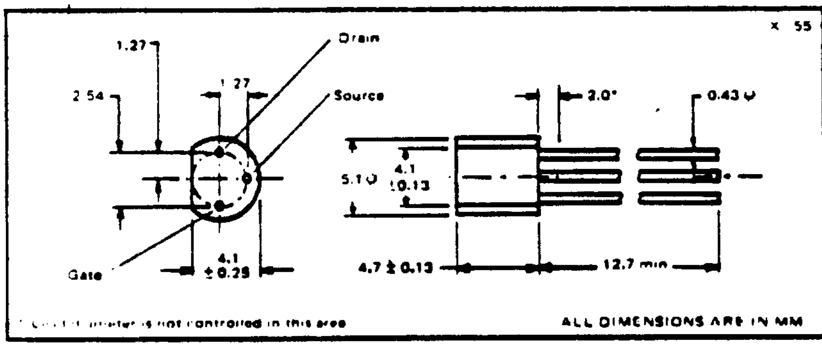
BF245
N-CHANNEL EPITAXIAL PLANAR SILICON FIELD EFFECT TRANSISTOR

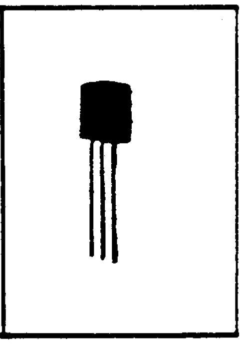
- VHF-Amplifiers and Mixer
- Common-Gate Circuits for Radio Frequency Application with Low Input Resistance and Small Feedback
- f_g = 700 MHz typ
- $1/g_{11s}$ = 4 kΩ
- $|Y_{21s}|$ = 5.5 mS typ
- C_{12s} = 1.1 pF typ

description

These components are tested according to the appropriate test method of MIL-STD-750. By special agreement, they can also be tested additionally to MIL or DIN specifications.

mechanical data





absolute maximum ratings at 25°C free air temperature (unless otherwise noted)

Drain-Gate Voltage	30 V
Drain-Source Voltage	±30 V
Gate Current	10 mA
Continuous Device Dissipation at 25°C Free Air Temperature (See Note 1)	300 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	260°C

NOTE: 1. Derate linearly to 150°C free air temperature at the rate of 2.4 mW/°C.

BF245
N-CHANNEL EPITAXIAL PLANAR SILICON FIELD EFFECT TRANSISTOR

electrical characteristics at 25°C free air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$-V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$-I_G = 1\ \mu A$, $V_{DS} = 0$	30			V
$-I_{GSS}$	Gate Reverse Current	$-V_{GS} = 20$ V, $V_{DS} = 0$ V			5	nA
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = 15$ V, $V_{GS} = 0$ V See Note 2	2		25	mA
$-V_{GS}$	Gate-Source Voltage	$V_{DS} = 15$ V, $I_D = 200\ \mu A$	0.4		7.5	V
$-V_{GS(off)}$	Gate-Source Cutoff Current	$V_{DS} = 15$ V, $I_D = 10$ nA	0.5		8.0	V
$\|Y_{21s}\|$	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = 15$ V, $-V_{GS} = 0$ V, f = 1 KHz	3.0	5.5	6.5	mS
f_g	Common-Source Bandwidth	$V_{DS} = 15$ V, $-V_{GS} = 0$ V, See Note 3		700		MHz
C_{12s}	Common-Source Short-Circuit Reverse Transfer Capacitance	$V_{DS} = 20$ V, $-V_{GS} = 1$ V, f = 1 MHz		1.1		pF
C_{11s}	Common-Source Short-Circuit Input Capacitance	$V_{DS} = 20$ V, $-V_{GS} = 1$ V, f = 1 MHz		4.0		pF
C_{22s}	Common-Source Short-Circuit Output Capacitance	$V_{DS} = 20$ V, $-V_{GS} = 1$ V, f = 1 MHz		1.6		pF
$1/g_{11s}$	Small Signal Common-Source Input Inpedance	$V_{DS} = 20$ V, $-V_{GS} = 1$ V, f = 100 MHz		14		kΩ
		$V_{DS} = 20$ V, $-V_{GS} = 1$ V, f = 200 MHz		4		kΩ

NOTES: 2. This value must be measured using pulse techniques: $t_p \leqslant 300\ \mu s$, duty cycle $\leqslant 2$ %.

3. Frequency at which the real part of the Forward Transfer Admittance has fallen by 3 dB refered to the value at 1KHz.

BF245
N-CHANNEL EPITAXIAL PLANAR SILICON FIELD EFFECT TRANSISTOR

On request following I_{DSS}/V_{GS}-Groups can be delivered

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 15 V, V_{GS} = 0 V	Group A	2.0	6.5	mA
			Group B	6.0	15	mA
			Group C	12	25	mA
$-V_{GS}$	Gate-Source Voltage	V_{DS} = 15 V, I_D = 200 µA	Group A	0.4	2.2	V
			Group B	1.6	3.8	V
			Group C	3.2	7.5	V

TYPE TIL100
LARGE-AREA SILICON PHOTODIODE

BULLETIN NO. DL-S 12631, MAY 1978–REVISED JULY 1978

- High Photosensitivity
- Fast Response
- Low-Cost Plastic Package
- Designed for Infrared Remote-Control Systems
- Spectrally Matched with TIL38 Emitter

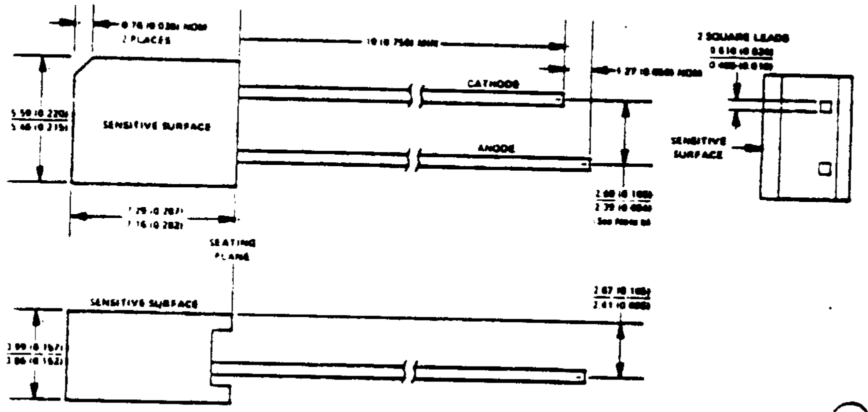
1

description

The TIL100 is a high-speed PIN photodiode designed to operate in the reverse-bias mode. It provides low capacitance with high speed and high photosensitivity suitable for near-infrared applications.

mechanical data

The photodiode chip is mounted on a lead frame and molded in a black infrared-transmissive plastic. The active chip area is typically 8,83 square millimeters (0.0137 square inches). Its centerline is nominally 4 millimeters (0.157 inch) above the seating plane.



NOTES: a. All dimensions are in millimeters and parenthetically in inches.
b. Lead spacing is measured at the seating plane.

8

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

6 Reverse Voltage	30 V
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	150 mW
7 Operating Free-Air Temperature Range	−25°C to 100°C
Storage Temperature Range	−25°C to 100°C
Lead Temperature 1,6 mm (1/16 inch) from Case for 3 Seconds	260°C

NOTE 1: Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.

TYPE TIL100
LARGE-AREA SILICON PHOTODIODE

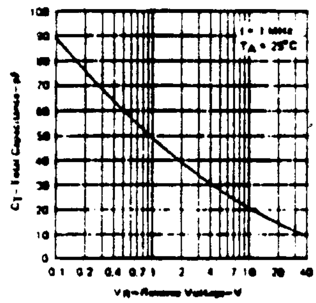
electrical characteristics at 25°C free-air temperature 1

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)}$	Breakdown Voltage	I_R = 100 μA,	E_e† = 0		30			V
I_D	Dark Current	V_R = 10 V,	E_e† = 0			5	2 50	nA
I_L	Light Current	V_R = 10 V,	E_e† = 2.5 μW/mm² at 940 nm		10	15		μA
5 C_T	Total Capacitance	V_R = 3 V,	E_e† = 0,	f = 1 MHz		30	50	pF
t_r	Rise Time	V_R = 10 V,	R_L = 1 kΩ			100		ns
t_f	Fall Time	V_R = 10 V,	R_L = 1 kΩ			100		ns

†Irradiance (E_e) is the radiant power per unit area incident on a surface.

TYPICAL CHARACTERISTICS

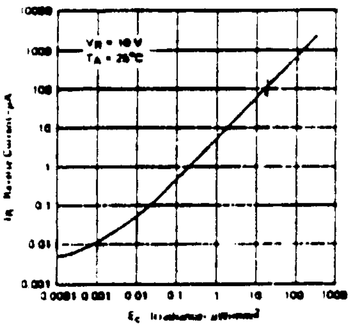
TOTAL CAPACITANCE
vs
REVERSE VOLTAGE



4

FIGURE 1

REVERSE CURRENT
vs
IRRADIANCE



3

FIGURE 2

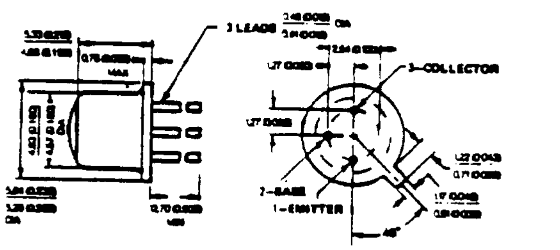
NPN PLANAR SILICON PHOTOTRANSISTORS

MARCH 1972 – REVISED AUGUST 1978

- Recommended for Application in Character Recognition, Tape and Card Readers, Velocity Indicators, and Encoders
- Spectrally and Mechanically Matched with TIL31/TIL33 IR-Emitters
- Glass-to-Metal-Seal Header
- Base Contact Externally Available
- Saturation Level Directly Compatible with Most TTL/DTL

mechanical data

The device is in a hermetically sealed package with glass window. The outline of the TIL81/TIL99 is similar to TO-18 except for the window. All TO-18 registration notes also apply to this outline.



THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE.

TIL81
MAXIMUM WINDOW EXTENSION FROM TOP OF CASE IS 1.78 (0.070). MINIMUM DIAMETER IS 3.18 (0.125).

TIL99
MAXIMUM WINDOW EXTENSION FROM TOP OF CASE IS 0.254 (0.010). MINIMUM DIAMETER IS 3.56 (0.140)

THE WINDOW IS CORNING 7052 GLASS (OR EQUIVALENT)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES UNLESS OTHERWISE NOTED.

10

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-Base Voltage	50 V
Collector-Emitter Voltage	30 V
Emitter-Base Voltage	7 V
Emitter-Collector Voltage	7 V
9 Continuous Collector Current	50 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	250 mW
Operating Free-Air Temperature Range	−65°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	240°C

NOTE 1: Derate linearly to 125°C free-air temperature at the rate of 2.5 mW/°C.

TYPES TIL81/TIL99
NPN PLANAR SILICON PHOTOTRANSISTORS

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

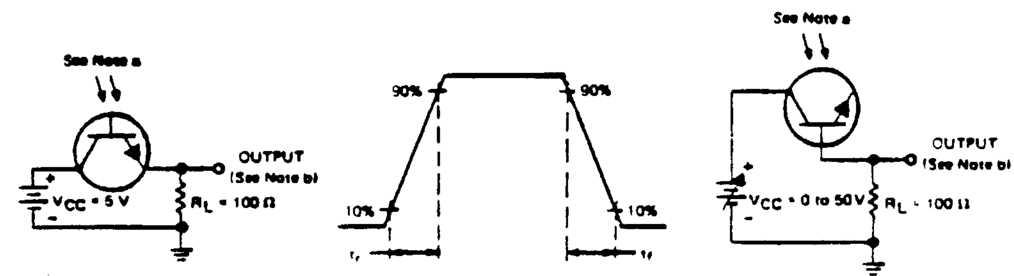
PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage			I_C = 100 μA, I_E = 0, H = 0	50			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage			I_C = 100 μA, I_B = 0, H = 0	30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage			I_E = 100 μA, I_C = 0, H = 0	7			V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage			I_E = 100 μA, I_B = 0, H = 0	7			V
I_D	Dark Current		Phototransistor Operation	V_{CE} = 10 V, I_B = 0, H = 0			0.1	
				V_{CE} = 10 V, I_B = 0, H = 0, T_A = 100 °C	(2)	20		μA
			Photodiode Operation	V_{CB} = 10 V, I_E = 0, H = 0			0.01	μA
I_L	Light Current	TIL 81	Phototransistor Operation	V_{CE} = 5 V, I_B = 0, H = 5 mW/cm², See Note 2	5	22		mA
			Photodiode Operation	V_{CB} = 0 to 50 V, I_E = 0, H = 20 mW/cm², See Note 2		170		μA
I_L	Light Current	TIL 99	Phototransistor Operation	V_{CE} = 5 V, I_B = 0, E_e = 20 mW/cm², See Note 2	1	5		mA
			Photodiode Operation	V_{CB} = 0 to 50 V, I_E = 0, E_e = 20 mW/cm², See Note 2		40		μA
h_{FE}	Static Forward Current Transfer Ratio			V_{CE} = 5 V, I_C = 1 mA, E_e = 0		300		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (8)			I_C = 0.4 mA, I_B = 0, E_e = 20 mW/cm², See Note 2		0.2		V

NOTE 2: Irradiance (E_e) is the radiant power per unit area incident upon a surface. For these measurements the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

switching characteristics at 25 °C free-air temperature (7)

PARAMETER			TEST CONDITIONS	TYPICAL	UNIT
t_r	Rise Time	Phototransistor Operation	V_{CC} = 5 V, I_L = 800 μA, R_L = 100 Ω, See Test Circuit A of Figure 1	8	μs
t_f	Fall Time			6	
t_r	Rise Time	Photodiode Operation	V_{CC} = 0 to 50 V, I_L = 60 μA, R_L = 100 Ω, See Test Circuit B of Figure 1	350	ns
t_f	Fall Time			500	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORM

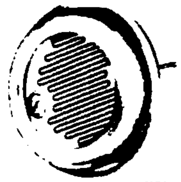
TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. Input irradiance is supplied by a pulsed gallium arsenide infrared emitter with rise and fall times less than 50 ns. Incident irradiation is adjusted for specified I_L.

b. Output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 25$ ns, $R_{in} \geq 1$ MΩ, $C_{in} \leq 20$ pF

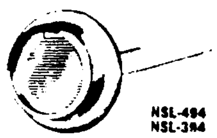
FIGURE 1

SUMMARY OF STANDARD PHOTOCELLS



NSL-446

NSL-467
NSL-367



NSL-494
NSL-394

NSL-464
NSL-364

NSL-487
NSL-387

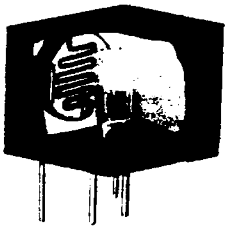
CADMIUM SULPHIDE PHOTOCONDUCTIVE CELLS (Peak of Spectral Response at 5500 Å)

Cell Type No.	1 Ftc Res. Kilohms**	Typical 100 Ftc Res. Ohms*	Min. Dark Res Megohms	Max Voltage Peak	Max. Power MW	Case Type
NSL-443	200	4500	300	2000	1000	Hermetic Glass and Metal 1.0" Dia. FIG. 4
NSL-444	120	2200	100	2000	1000	
NSL-445	26.0	550	40	420	1000	
NSL-446	11.4	200	12	420	1000	
NSL-447	5.5	140	2.3	420	1000	
NSL-461	65	1500	30	70	100	Hermetic Glass and Metal 0.250" Dia. FIG. 5
NSL-462	28	600	20	70	100	
NSL-463	12	340	2.7	70	100	
NSL-464	5.2	180	0.7	70	100	
NSL-465	550	12000	160	250	100	
NSL-466	230	6600	20	250	100	
NSL-467	100	2400	[illegible]	250	100	
NSL-481	43	1000	55	120	200	Hermetic Glass and Metal TO-5 FIG. 6
NSL-482	18.6	400	15	120	200	
NSL-483	8	230	1.8	120	200	
NSL-484	3.5	120	0.25	120	200	
NSL-487	160	4600	130	250	200	
NSL-491	9.3	210	14	70	500	Hermetic Glass and Metal TO-8 FIG. 7
NSL-492	4.0	80	3.2	70	500	
NSL-493	1.7	50	0.4	70	500	
NSL-494	0.75	30	0.05	70	500	
NSL-495	40	860	32	350	500	
NSL-496	17	500	4.0	350	500	
NSL-497	7.5	260	0.54	350	500	
NSL-4931	1.7	50	0.4	70	200	Epoxy 0.5" Dia. FIG. 8
NSL-4961	17.0	500	4.0	350	200	

CADMIUM SELENIDE PHOTOCONDUCTIVE CELLS (Peak of Spectral Response at 7200 Å)

Cell Type No.	1 Ftc Res. Kilohms**	Typical 100 Ftc Res. Ohms**	Min. Dark Res. Megohms	Max Voltage Peak	Max. Power MW	Case Type
NSL-364	5.2	125	200	80	100	Hermetic 0.250" Dia. FIG. 5
NSL-367	100	2400	3000	250	100	
NSL-384	3.5	90	100	80	100	Hermetic TO-5 FIG. 6
NSL-387	68	1600	1000	250	100	
NSL-393	1.7	40	10	80	500	Hermetic TO-8 FIG. 7
NSL-396	17.0	400	100	320	500	
NSL-3931	1.7	40	2.0	70	200	Epoxy 0.5" Dia. FIG. 8
NSL-3961	17.0	400	20.0	350	200	

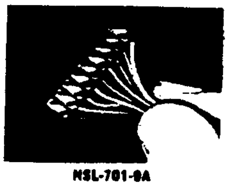
**Source at 2870°K



PL-1036-1

PHOTOCELL - LAMP ASSEMRLIES

Type No	Lamp Volts	Lamp Current MA	Max. On Res. Ohms	Min. OFF Res. Megohms	Max. Volts	Max. Power MW	Case Type
PL-1033-1	10	15	100	10	80	250	Phenolic .75" x .75" x .625" Pin Leads for P.C. Board Mounting FIG. 9
PL-1036-1	10	15	400	100	320	250	
PL-1033-2	10	15	Dual Photocell Unit 100	10	80	250	
PL-1036-2	10	15	Dual Photocell Unit 400	100	320	250	
PL-2H33-1	120	2	100	10	80	250	
PL-2H36-1	120	2	400	100	320	250	
PLT-10384	10	15	400	10	80	100	Tubular Axial Leads FIG. 10
PL-1036-2TR	Special Dual Tracking Unit		Res. at 3.5v - 7-20K Ohms Tracking ±20% Res. at 10v - 1.5K Ohms Max. Off R. 10 Megs				Otherwise same as PL-1036-2



NSL-701-9A

SILICON PHOTODIODES (Peak of Spectral Response at 8600 Å)

Type No.	Min. Short Ckt. Current MA*	Min. Open Ckt Voltage*	Max Reverse Dark Current	Max Reverse Volts	Description
NSL-701-1	0.30	0.35	10 µA	5	Silicon Chip .1" x .2" Coated, wire leads FIG. 11
NSL-701-9A	0.30	0.35	10 µA	5	Nine element cell 0.1" spacing, wire leads FIG. 12
NSL-703	1.5	0.42	50 µA	5	Silicon chip .2" x .4" Coated, wire leads FIG. 13
NSL-710P	0.125	0.40	2 µA	5	TO-18 Package FIG. 14
NSL-720	0.100	0.30	1 µA	5	TO-5 Package FIG. 15
NSL-820	0.125	0.25	0.5 µA	15	TO-5 Package Special Low Capacitance Low Noise Unit FIG. 15

* . . . at 500 Ftc (25 MW/cm²) 2800°K Source

SILICON PHOTOTRANSISTOR (Peak of Spectral Response at 8600 Å)

Type No.	I_{CEO}* at 15V	Dark I_{CEO} at 25°C	Max. Voltage V_{CEO}	Power Rating MW	Description
PT-701	.5 MA	.05 µA	30	150	NPN Silicon Transistor TO-18 Case FIG. 16

* . . . at 200 Ftc (10 MW/cm²) 2800°K Source

PTC Thermistors

PTC thermistors as temperature sensor for measurement and control tasks

Reference temperature T_{ref} °C	Reference resistance R_{ref} Ω	Temperature T_P °C	Resistance value at T_P R_P kΩ	Ordering code	Min. qty.	to 49	50 to 99	100 to 499	500 to 999
Operating voltage V_{max} = 10 V									
60	12	110	≥ 4	Q63100-P330-C14	10				
80	12	125	≥ 4	Q63100-P350-C14	10				
120	12	155	≥ 4	Q63100-P390-C14	10				
Operating voltage V_{max} = 30 V									
0	1200	60	≥ 200	Q63100-P270-C11	10				
40	190	95	≥ 50	Q63100-P310-C11	10				
60	160	110	≥ 50	Q63100-P330-C11	10				
80	160	125	≥ 50	Q63100-P350-C11	10				
120	150	155	≥ 50	Q63100-P390-C11	10				
Operating voltage V_{max} = 50 V									
40	220	95	≥ 50	Q63100-P310-C12	10				
60	160	110	≥ 50	Q63100-P330-C12	10				
80	160	125	≥ 50	Q63100-P350-C12	10				
120	170	155	≥ 50	Q63100-P390-C12	10				
Operating voltage V_{max} = 60 V									
60	54	110	≥ 20	Q63100-P330-C13	10				
80	54	125	≥ 20	Q63100-P350-C13	10				
120	58	155	≥ 20	Q63100-P390-C13	10				
Operating voltage V_{max} = 250 V									
60	2000	110	≥ 1	Q63100-P330-C40	10				
80	2000	125	≥ 1	Q63100-P350-C40	10				
120	2000	155	≥ 1	Q63100-P390-C40	10				
Operating voltage V_{max} = 20 V; Test voltage leads/case 220 Vac									
60	160	110	≥ 100	Q63100-P330-D1	5				
80	152	125	≥ 100	Q63100-P350-D1	5				
120	148	155	≥ 100	Q63100-P390-D1	5				
Operating voltage V_{max} = 20 V; Test voltage leads/case 3 kVac									
40	230	95	≥ 100	Q63100-P310-D401	5				
60	160	110	≥ 100	Q63100-P330-D401	5				
80	152	125	≥ 100	Q63100-P350-D401	5				
90	152	130	≥ 100	Q63100-P360-D401	5				
120	148	155	≥ 100	Q63100-P390-D401	5				

For dimensional drawings refer to page 10.5

PTC Thermistors

PTC thermistors as temperature sensor for measurement and control tasks

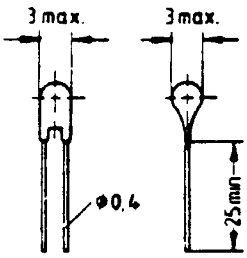
Nominal threshold temperature T_{NAT}[1] °C	PTC resistance T_{amb} = 25 °C Ω	PTC temperature: T_{NAT-T} Ω	T_{NAT+T} Ω	Ordering code	Min. qty.	to 49	50 to 99	100 to 499	500 to 999
Operating voltage V_{max} = 25 V									
▼ 60	≤ 250	≤ 570	≥ 570	Q63100-P331-C8	10				
▼ 70	≤ 250	≤ 570	≥ 570	Q63100-P341-C8	10				
▼ 80	≤ 250	≤ 570	≥ 570	Q63100-P351-C8	10				
▼ 90	≤ 250	≤ 550	≥ 1330	Q63100-P361-C8	10				
▼ 100	≤ 250	≤ 550	≥ 1330	Q63100-P371-C8	10				
▼ 110	≤ 250	≤ 550	≥ 1330	Q63100-P381-C8	10				
▼ 120	≤ 250	≤ 550	≥ 1330	Q63100-P391-C8	10				
▼ 130	≤ 250	≤ 550	≥ 1330	Q63100-P401-C8	10				
▼ 140	≤ 250	≤ 550	≥ 1330	Q63100-P411-C8	10				
▼ 145	≤ 250	≤ 550	≥ 1330	Q63100-P416-C8	10				
▼ 150	≤ 250	≤ 550	≥ 1330	Q63100-P421-C8	10				
▼ 155	≤ 250	≤ 550	≥ 1330	Q63100-P426-C8	10				
▼ 160	≤ 250	≤ 550	≥ 1330	Q63100-P431-C8	10				
▼ 170	≤ 250	≤ 550	≥ 1330	Q63100-P441-C8	10				
▼ 180	≤ 250	≤ 550	≥ 1330	Q63100-P451-C8	10				
Operating voltage V_{max} = 30 V									
60	≤ 100	≤ 570	≥ 570	Q63100-P331-C100	10				
70	≤ 100	≤ 570	≥ 570	Q63100-P341-C100	10				
80	≤ 100	≤ 570	≥ 570	Q63100-P351-C100	10				
90	≤ 100	≤ 550	≥ 1330	Q63100-P361-C100	10				
100	≤ 100	≤ 550	≥ 1330	Q63100-P371-C100	10				
110	≤ 100	≤ 550	≥ 1330	Q63100-P381-C100	10				
120	≤ 100	≤ 550	≥ 1330	Q63100-P391-C100	10				
130	≤ 100	≤ 550	≥ 1330	Q63100-P401-C100	10				
140	≤ 100	≤ 550	≥ 1330	Q63100-P411-C100	10				
145	≤ 100	≤ 550	≥ 1330	Q63100-P416-C100	10				
150	≤ 100	≤ 550	≥ 1330	Q63100-P421-C100	10				
155	≤ 100	≤ 550	≥ 1330	Q63100-P426-C100	10				
160	≤ 100	≤ 550	≥ 1330	Q63100-P431-C100	10				
170	≤ 100	≤ 550	≥ 1330	Q63100-P441-C100	10				
180	≤ 100	≤ 550	≥ 1330	Q63100-P451-C100	10				
Operating voltage V_{max} = 30 V									
▼ 60	≤ 100	≤ 570	≥ 570	Q63100-P331-D801	10				
▼ 70	≤ 100	≤ 570	≥ 570	Q63100-P341-D801	10				
▼ 80	≤ 100	≤ 570	≥ 570	Q63100-P351-D801	10				
▼ 90	≤ 100	≤ 550	≥ 1330	Q63100-P361-D801	10				
▼ 100	≤ 100	≤ 550	≥ 1330	Q63100-P371-D801	10				
▼ 110	≤ 100	≤ 550	≥ 1330	Q63100-P381-D801	10				
▼ 120	≤ 100	≤ 550	≥ 1330	Q63100-P391-D801	10				
▼ 130	≤ 100	≤ 550	≥ 1330	Q63100-P401-D801	10				
▼ 140	≤ 100	≤ 550	≥ 1330	Q63100-P411-D801	10				

[1]) Tolerance T_{NAT} = ±5 K

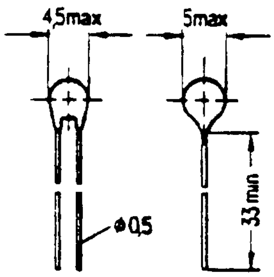
PTC Thermistors

PTC thermistors as temperature sensors for measurement and control tasks
Dimensional drawings

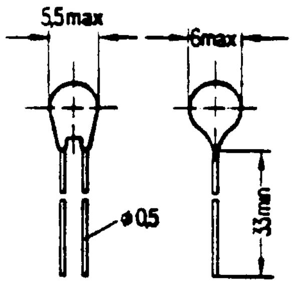
Q63100–P*-C8**
(encapsulated)



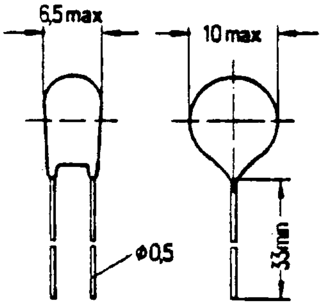
Q63100–P*-C11**
(encapsulated)



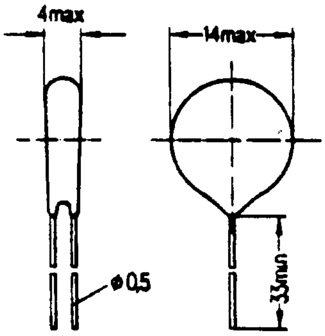
Q63100–P*-C12**
(encapsulated)



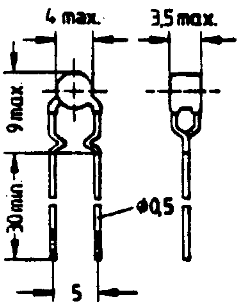
Q63100–P*-C13**
(encapsulated)



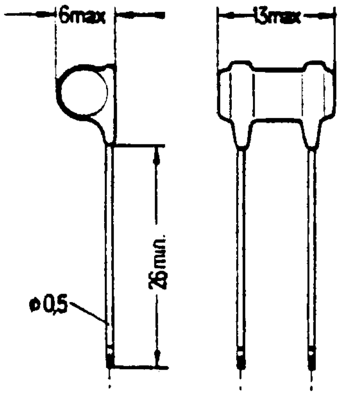
Q63100–P*-C14**
(encapsulated)



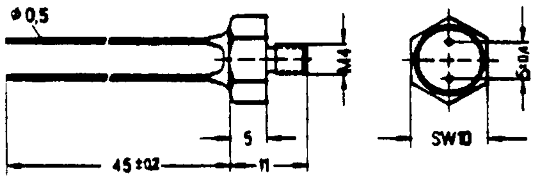
Q63100-P*-C100**
(encapsulated)



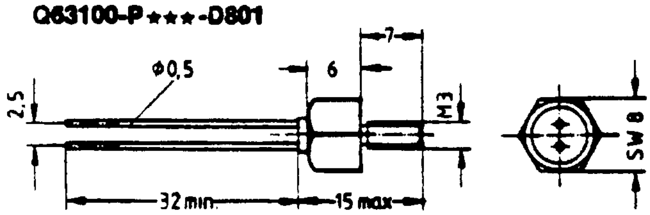
Q63100–P*-C40 (encapsulated)**



Q63100–P*-D1, -D401**
(incorporated in a screw-type case, electrically insulated)



Q63100-P*-D801**



Dimensions in mm

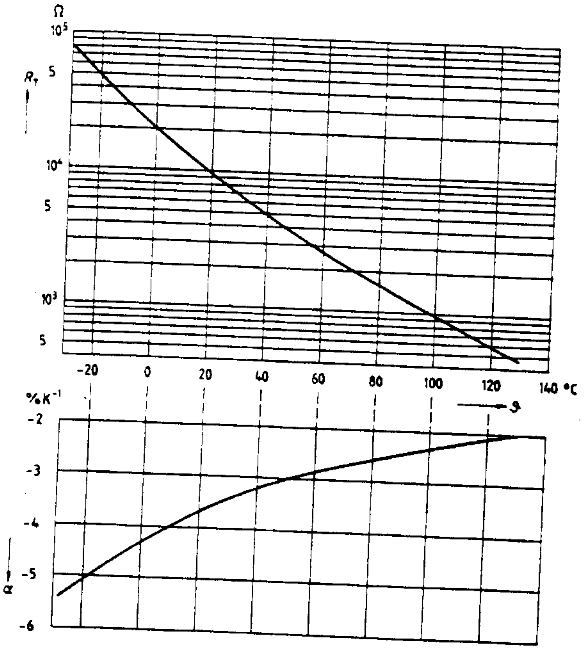
Generalità

I termistori NTC sono resistenze a semiconduttori con coefficiente di temperatura negativo (compreso tra 3 e 5%/K), realizzati mediante stampaggio e successiva sinterizzazione degli ossidi dei metalloidi manganese, ferro, cobalto, rame, nichel e zinco.
Già da tempo i termistori hanno trovato ampia applicazione nel settore dell'elettronica grazie alle loro eccellenti caratteristiche quali:

- Elevata sensibilità
- Buona riproducibilità grazie alla stabilità meccanica, termica ed elettrica
- Resistenza agli influssi esterni
- Lunga durata
- Ingombro ridotto
- Rapporto prezzo/prestazioni

La semplicità d'impiego e l'elevata affidabilità li rendono particolarmente adatti a compiti di controllo, sorveglianza, misura e simili.

Il rapporto tra resistenza e temperatura si rileva dalla caratteristica R/T e dal coefficiente di temperatura.



Compensazione della temperatura

Quasi tutti i semiconduttori hanno un coefficiente di temperatura positivo, per cui i termistori consentono di stabilizzare, a costi contenuti, la temperatura dei circuiti elettronici (equipaggiati con termistori SIPMOS, tiristori di potenza, TRIACS) che possono quindi funzionare senza subire l'influsso della temperatura ambiente e della potenza dissipata. In questo caso è importante l'accoppiamento termico tra NTC e componenti da compensare in modo che la caratteristica d'intervento risulti sincrona. Se la temperatura deve avere un andamento lineare, è sufficiente collegare una resistenza in parallelo o un circuito di linearizzazione; la funzione che ne deriva presenta un andamento sinusoidale, per cui la temperatura nel punto d'inversione deve trovarsi al centro del campo della temperatura di lavoro. Il valore della resistenza in parallelo si deduce dalla seguente formula:[1]

$R_p = R_{TM} \times (B - 2\ TM) / (B + 2\ TM)$

R_p = Resistenza in parallelo
R_{TM} = Resistenza del termistore al centro di un campo di temperatura
TM = Temperatura al centro di un campo di temperatura
B = Coefficiente B del termistore

Per dimensionare i circuiti, è opportuno dire che gli NTC a più bassa resistenza presentano un coefficiente B minore, per cui sono adatti a campi di temperatura più ampi, quelli a più alta resistenza hanno invece un coefficiente B più elevato e quindi sono adatti a circuiti maggiormente sensibili alla temperatura.

È disponibile una vasta gamma di NTC per i più svariati casi, per esempio il termistore K 45 è idoneo al montaggio su dissipatori di calore, il C 621 (formato chip) è stato studiato per il montaggio automatizzato.

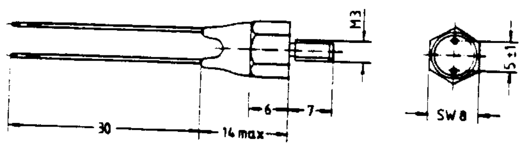
Esempi d'impiego

- **Nell'elettronica civile**
  Compensazione della temperatura negli stadi finali Hi-Fi equipaggiati con transistori SIPMOS, circuiti di sintonia AF con diodi capacitivi ecc.
- **Nell'elettronica industriale**
  Stabilizzazione della temperatura di diodi laser e fotoelementi con refrigeratore PELTIER, caricabatterie a celle solari, compensazione del giunto freddo di termocoppie, compensazione della temperatura di bobine di rame ecc.
- **Negli elettrodomestici**
  Stabilizzazione della velocità in apparecchi da cucina, fruste miscelatrici ecc.

1) Su richiesta è disponibile un programma computerizzato per ottimizzare il circuito di linearizzazione.

Compensazione della temperatura

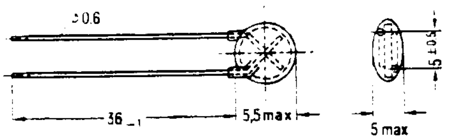
K 45



Tipo	Resistenza nominale R_N Ω	Tolleranza ΔR_N %	Coefficiente B K	Carico ammissibile P_{25} (ϑ_u = 25 °C) mW
K 45 da 6,8Ω a 470 kΩ	6,8	±10	2600	750
	10		2600	
	15		2900	
	22		2900	
	33		2900	
	47		3000	
	68		3050	
	100		3200	
	150		3200	
	220		3200	
	330		3450	
	470		3450	
	680		3560	
	1,0 k		3700	
	1,5 k		3900	
	2,2 k		3900	
K 164 da 6,8Ω a 470 kΩ	3,3 k	±10	3950	
	4,7 k	±20	3950	
	6,8 k		4200	
	10 k		4300	
	15 k		4150	
	22 k		4300	
	33 k		4300	
	47 k		4450	
	68 k		4600	
	100 k		4600	
	150 k		4600	
	220 k		4830	
	330 k		4850	
	470 k		4850	

* Al posto dell'asterisco bisogna mettere la lettera relativa alla tolleranza richiesta: K ≙ ± 10%, M ≙ ± 20%

K 164



Temperatura nominale ϑ_N °C	Campo di temperatura secondo DIN 40 040 °C	Costante termica del tempo di raffreddamento τ_{th} s	Sigla di ordinazione Tipo K 45 Q63045-	Tipo K 164 Q63016-
25	da −55 a +125	ca. 30	-K60-K800	-K4006-*8
			-K100-K	-K4010-*
			-K150-K	-K4015-*
			-K220-K	-K4022-*
			-K330-K	-K4033-*
			-K470-K	-K4047-*
			-K680-K	-K4068-*
			-K101-K	-K4100-*
			-K151-K	-K4150-*
			-K221-K	-K4220-*
			-K331-K	-K4330-*
			-K471-K	-K4470-*
			-K681-K	-K4680-*
			-K102-K	-K4001-*40
			-K152-K	-K4001-*45
		20 (±5)	-K222-K	-K4002-*42
			-K332-K	-K4003-*43
			-K472-K	-K4004-*47
			-K682-K	-K4006-*48
			-K103-K	-K4010-*40
			-K153-K	-K4015-*40
			-K223-K	-K4022-*40
			-K333-K	-K4033-*40
			-K473-K	-K4047-*40
			-K683-K	-K4068-*40
			-K104-K	-K4100-*40
			-K154-K	-K4150-*40
			-K224-K	-K4220-*40
			-K334-K	-K4330-*40
			-K474-K	-K4470-*40

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