The Field Effect Transistor

1. Introduction

The Field Effect Transistor (FET) has a long story from concept to the first physical implementation. The idea of a field effect transistor was first presented and patented in 1926 by the physicist Julius Edgar Lilienfeld. In 1935, the electrical engineer and inventor Oskar Heil described the possibility of controlling the resistance in a semiconducting material with an electric field in a British patent. A team from Bell Labs formed by John Bardeen and Walter Houser Brattain under the supervision of William Shockley observed and described the transistor effect in 1947. Their trying to build a working FET was unsuccessful, but they accidentally discovered the point-contact transistor. This epochal invention was followed by Shockley's bipolar junction transistor (BJT) in 1948.
In 1945, Heinrich Welker patented for the first time a Junction Field Effect Transistor (JFET). A Japanese team formed by Y. Watanabe and professor Jun-Ichi Nishizawa of Tohoku University patented the Static Induction Transistor (SIT) in 1950. The device controlled current flow by means of the static induction or electrostatic field surrounding two opposed gates (it was conceived as a solid-state analog of the vacuum-tube triode, and the first SIT's were produced in 1970 by several Japanese companies).
In 1952 William Shockley presented theoretical aspects regarding the JFET structure and its operation. Then, the first JFET was produced as a practical device by George Clement Dacey and Ian Munro Ross from Bell Labs in 1953, under the supervision of William Shockley.
In 1959, Mohamed M. Atalla and Dawon Kahng from Bell Labs invented the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This is the basic component used in digital electronics, and is the most frequently manufactured device in the history (about 1.3×10^{22} MOSFETs were manufactured between 1960 and 2018).

2. FET brief theory

Currently, there are two types of Field Effect Transistors (FET's) that are manufactured on a large scale: the Junction Field Effect Transistor (JFET) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The basic material used to produce these transistors is silicon. Depending on the impurities introduced into the silicon in the manufacturing process, there are 2 types of field effect transistors: with n channel and with p channel. Thus, a single type of charge carriers will circulate through a device: electrons for n-channel transistors, and holes for p-channel transistors. For this reason the field effect transistors are called unipolar devices. Because the mobility of the electron is greater than the mobility of the hole, n-channel transistors (through which the electrons flow) are faster than p-channel transistors (through which the holes flow), and therefore are manufactured in greater numbers.

a. The Junction Field Effect Transistor (J-FET)

The JFET is a three terminal device, which presents an area of doped silicon (n-type for n-channel JFET, p-type for p-channel JFET) with two diffusions of the opposite doping (p-type diffusion for n-channel JFET, n-type diffusion for n-type JFET). To allow a symmetrical control of the flow of electrical charges through the channel, the flow control electrode (the gate) is built on both sides of the channel and it is connected to the opposite doping areas (Fig.1).

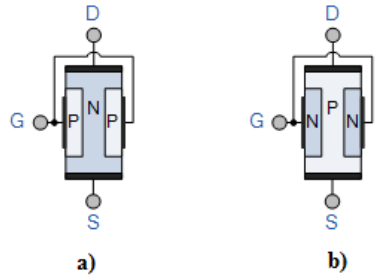


Fig.1.The internal structure for a JFET: a) n-channel J-FET; b) p-chanel J-FET
The terminals are: D-Drain; S-Source; G-Gate

The symbols for the n and p channel JFETS are represented in Fig.2. Although the J-FET is a symmetric device (the source and the drain may be interchanged), there are some situations when, for a discrete component, reversing the terminals (D and S) can damage the device. This can be identified by consulting the part datasheet given by the manufacturer. The drain and the source are connected at either end of the channel region.

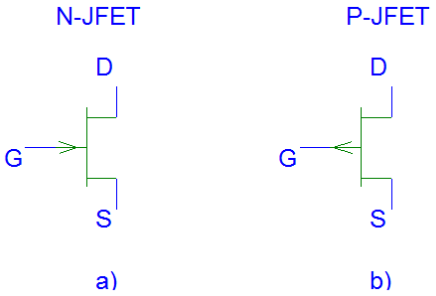


Fig.2.The electrical symbol for the JFET: a) n-channel J-FET; b) p-chanel J-FET
The terminals are: D-Drain; S-Source; G-Gate

The JFET operation is based on changing the drain current (I_D) as a function of the bias voltage applied on the *pn* junction between the gate and the channel (V_{GS}) (Fig.3). Because the gate contacts are internally connected, we have two *pn* junctions in parallel. The *pn* junctions are in reverse bias, so the gate current is very small (order of pico-amps, $I_G \approx 0$).

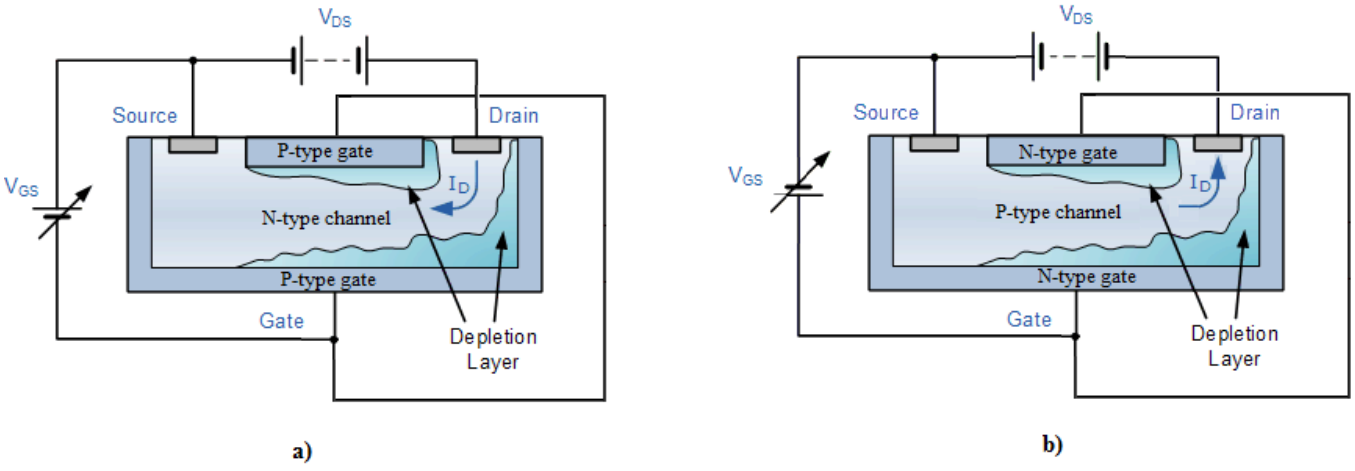


Fig.3.The DC bias for J-FET transistor: a) n-channel J-FET; b) p-channel J-FET

For optimal operation, the transistor needs to be biased from two external DC voltage sources: a drain-source

voltage source (V_{DS}) and a gate-source voltage source (V_{GS}). The V_{GS} source has an inverse polarity compared to the V_{DS} source. When a voltage is applied between the drain and the source, the current will flow through the channel. By changing the V_{GS}, the thickness of the channel is adjusted, and therefore a greater or lesser number of electrical charges (electrons for n-JFET, or holes for p-JFET) will pass through the channel, starting from the source to the drain. If V_{GS}=0V, the device is in a normally on state and a maximum number of electrical charges will pass through the channel. To decrease the drain current, we must apply an appropriate voltage to the gate and use the depletion region created at the junction to control the channel width. In conclusion, it can be seen that the JFET is a voltage controlled device. The drain and the source currents are equal (I_D=I_S) (Fig.4).

1. *Effects on changing V_{GS} (V_{DS}=ct)*

In Fig.4 is represented the schematic diagram with a JFET biased from 2 voltage sources: a constant and small V_{DS} (the width of the channel is almost constant), and a variable V_{GS}. The increasing width of the pn junction depletion region (illustrated from yellow to red to blue), is due to the increasing reverse bias of the junction resulting from the application of a $|V_{GS}|$ of increasing magnitude. As the depletion widths increase, the channel width decreases, resulting in a lower conductivity (higher resistivity) of the channel. As $|V_{GS}|$ is increased, a value of V_{GS} is reached for which the channel is completely depleted (no free carriers) and no current will flow regardless of the applied V_{DS}. This is called the **threshold**, or **pinch-off**, **voltage** and occurs at V_{GS}= V_T = V_P. The threshold voltage is negative for a n-channel JFET(V_p < 0) and positive for a p-channel JFET(V_p > 0) .

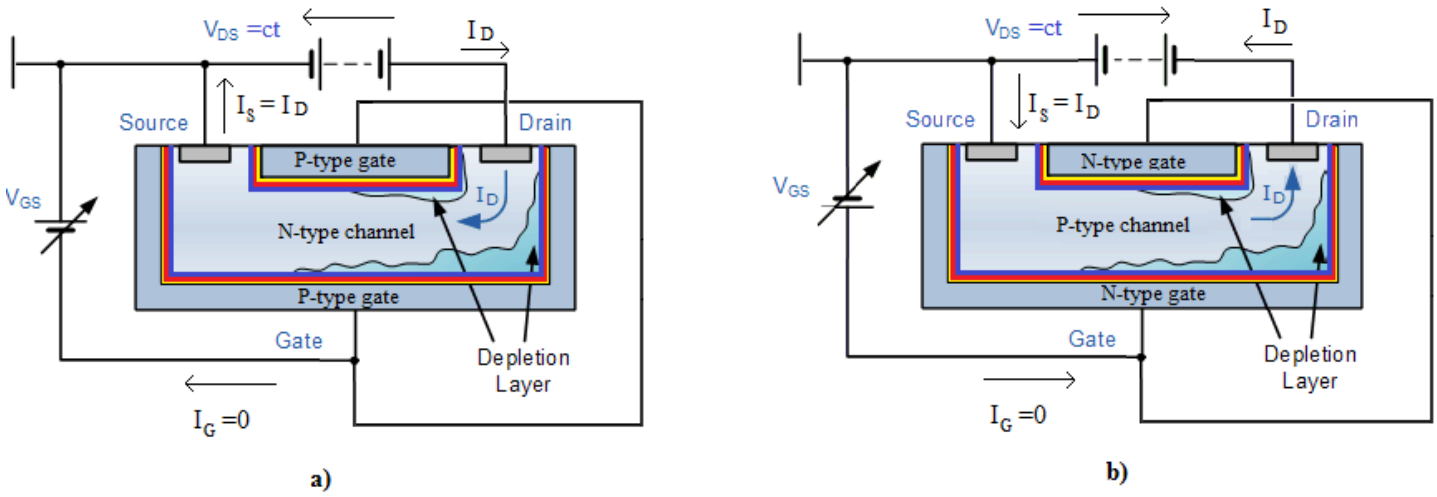


Fig.4.The DC bias analysis at variable V_{GS} for J-FET transistor: a) n-channel J-FET; b) p-channel J-FET

2. *Effects on changing V_{DS} (V_{GS}=0)*

In Fig.5 is represented the circuit which bias the JFET with a variable V_{DS} while V_{GS}=0V. The V_{DS} voltage is positive for a n-channel JFET and negative for a p-channel JFET. We assume a constant doping so that the voltage variation in the channel is linear. When V_{DS} is very small, the voltage variation in the channel is very small and it has no effect on the channel shape. For this case, the depletion region is only due to the pn junction as shown in yellow in the figure. As $|V_{DS}|$ increases, the increasing potential at the drain reverse biases the pn junctions. Since the voltage drop across the channel increases from source to drain, the reverse bias of the pn junction also increases from source to drain. Since the depletion region is a function of bias, the depletion region also gets wider from source to drain, causing the channel to become tapered as shown in red in the figure. The current still increases with increasing V_{DS}, however there is no longer a linear relationship between V_{DS} and I_D since the channel resistance is a function of its width. Further increases in V_{DS}, for example, blue in the figure, result in a more tapered shape to the channel and increasing nonlinearities in the I_D - V_{DS}

relationship. This process continues until a V_{DS} is reached where the depletion regions from the pn junctions merge. Analytically, this occurs when the gate-to-drain voltage V_{GD} is less than some threshold $V_T=V_p$ and is known as the **pinch-off point**. At this point, the drain current saturates and further increases in V_{DS} result in little (ideally zero) change in I_D. For the case $v_{GG}=v_{GS}=0$, the drain current at pinch-off is called the **drain-source saturation current - I_{DSS}**. Operation beyond the pinch-off point ($V_{DS}>|V_{GS}=V_P|$) defines the **normal operating** or **saturation region** of the JFET.

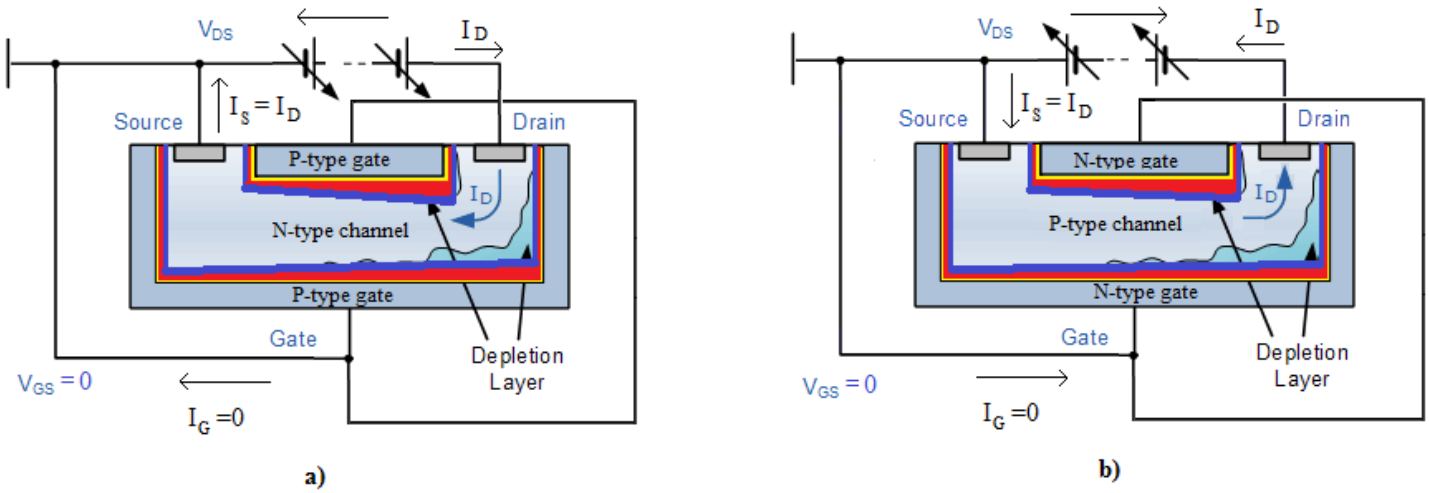


Fig.5.The DC bias analysis at a variable V_{DS} and V_{GS} =0 for J-FET transistor:
a) n-channel J-FET; b) p-channel J-FET

If the V_{DS} variation effect is applied, we can see that pinch-off will occur for lower values of V_{DS} since we have less of a channel to start with (resulting in lower values of I_D at pinch-off). By combining the effect of V_{DS} and V_{GS} variations, a family of characteristic curves will be generated for the JFET (Fig.6).

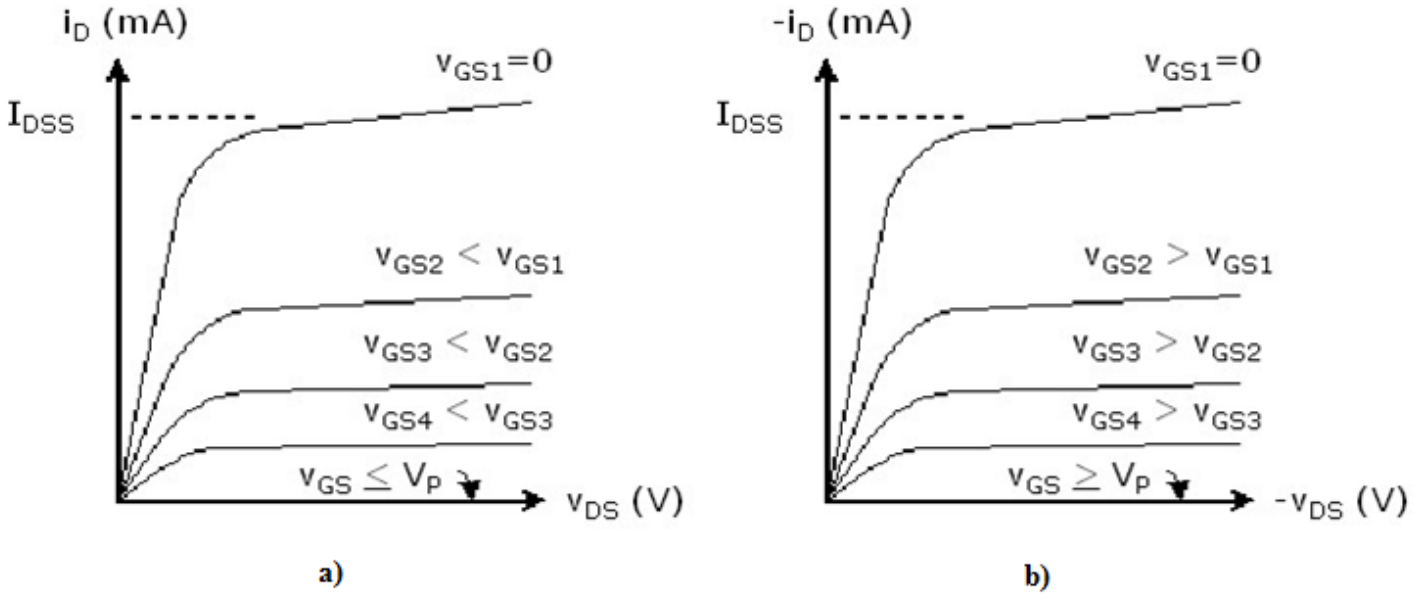


Fig.6.The DC output characteristics at a variable V_{DS} and several values of V_{GS} =ct for J-FET transistor:
a) n-channel J-FET; b) p-channel J-FET

The output characteristic for a n-channel J-FET with detailed explanations is presented in Fig.7. After the JFET reaches saturation, I_D remains relatively constant with a very small slope for further increases in V_{DS} (the slope of the curves would be zero for an ideal device).

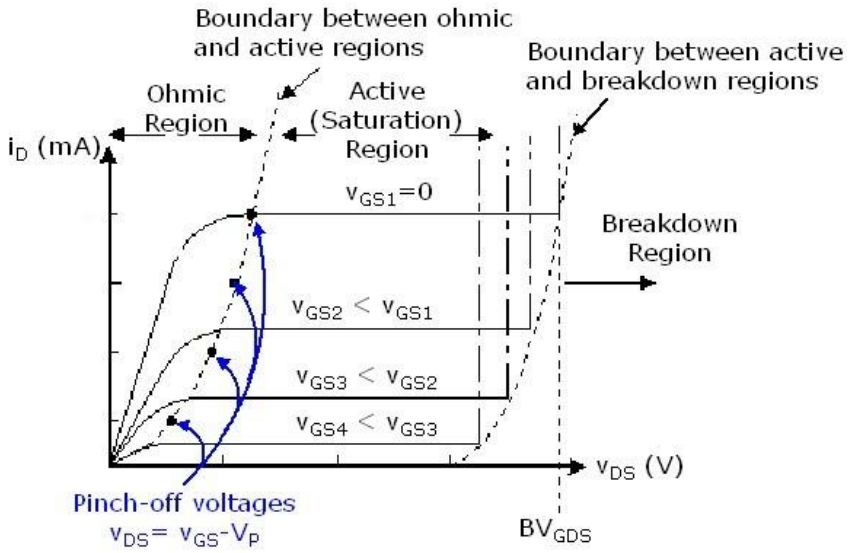


Fig.7.The complete DC output characteristics for n-channel J-FET

The transfer characteristics for n and p channel JFET's are presented in Fig. 8.

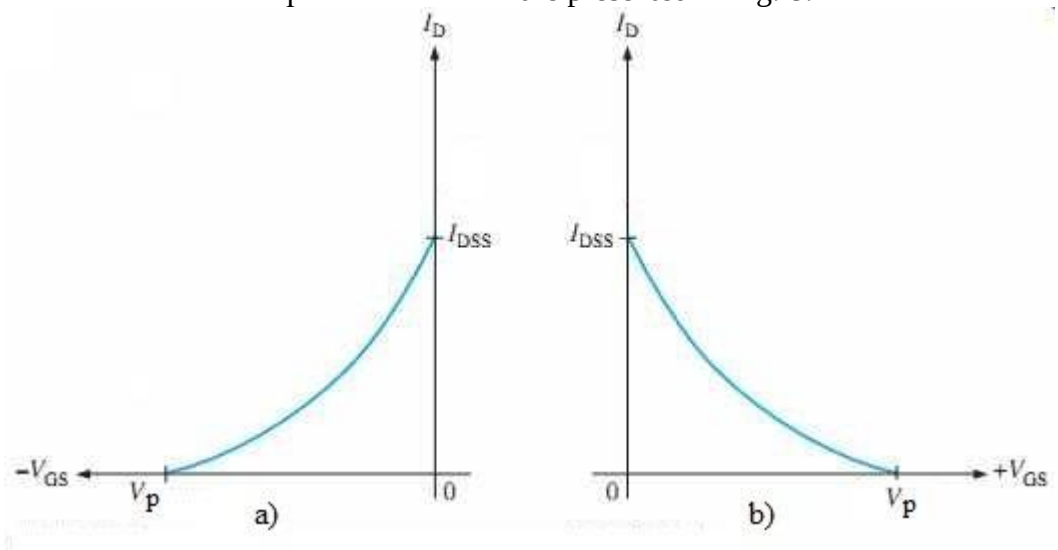


Fig.8.The transfer characteristics for J-FET: a) n-channel J-FET; b) p-channel J-FET

Below pinch-off, the channel essentially behaves like a constant resistance. This linear region of operation is called **ohmic** (or sometimes triode), and is where the JFET may be used as a voltage controlled resistor (the control voltage in V_{GS}). As the magnitude of V_{GS} increases, the range of V_{DS} where the transistor may be operated as an ohmic resistor decreases. In the ohmic region, the potentials at all three terminals strongly affect the drain current. The drain current is:

$$I_D = I_{DSS}\left[2\left(\frac{V_{GS}}{V_P}-1\right)\frac{V_{DS}}{V_P}-\left(\frac{V_{DS}}{V_P}\right)^2\right] \quad (1)$$

Beyond the knee of the ohmic region, the curves become essentially flat in the **active** (or **saturation**) **region** of operation. The transistor may be used as an amplifier in this region. To **operate in the linear region**, it is standard practice to **define the dc bias current as between 30% and 70% of I_{DSS}.** This locates the DC operating point in the most linear region of the characteristic curves.

The drain current in the saturation region may be defined by using the Shockley equation:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \cdot \left(1+\lambda \cdot V_{DS}\right) \tag{2}$$

The λ is known as the channel length modulation parameter. Usually, especially for large-signal analysis or biasing, λ is small enough that $|\lambda \cdot V_{DS}| << 1$. The parameters I_{DSS} and V_P (sometimes called V_T or $V_{GS(OFF)}$ on the data sheets) are generally given by the manufacturer.

The JFET small signal AC model at low frequencies

The AC small signal model for low frequencies (below 10KHz) of the JFET is given in Fig.9. The transconductance (g_m) and the output resistance of the device (r_o) are:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)\left(1+\lambda V_{DS}\right) \tag{3}$$

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \cdot \lambda} \tag{4}$$

The channel length modulation parameter may be neglected in some situations.

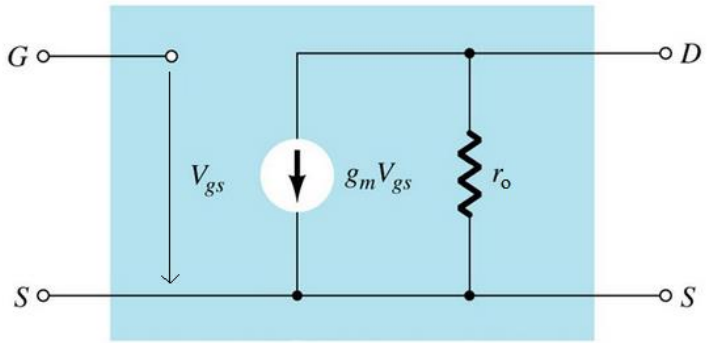


Fig.9.The AC equivalent circuit for J-FET

b. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The MOSFET is a device with four terminals. It has a source (S) and a drain (D), two highly conducting n-type semiconductor regions which are isolated from the p-type substrate (SB) by reversed-biased p-n diodes. A metal (or poly-crystalline) gate (G) covers the region between source and drain, but is separated from the semiconductor by a high quality gate oxide (SiO_2). The basic structure of a MOSFET and the corresponding circuit symbol are shown in Fig.10. The source and the drain regions are identical. The source provides the electrical charges (electrons for n-MOS, holes for p-MOS), while the other n-type region (the drain) collects the electrical charges (electrons for n-MOS, holes for p-MOS). The voltages applied to the drain and gate electrode as well as to the substrate by means of a back contact are referred to the source potential, as also indicated on the figure. By applying a potential between the gate (G) and the source (S) terminals, the flow of the electrical charges from the source to the drain may be controlled.

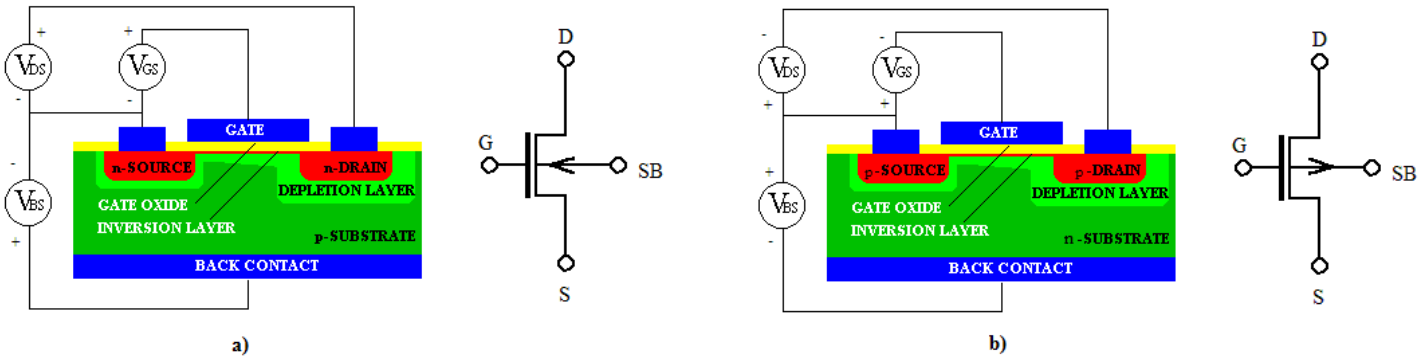


Fig.10.The DC biasing and the symbols for the MOSFET transistor:
a) n-channel MOSFET; b) p-channel MOSFET

For the discrete MOSFET transistors which are commercially available, the substrate (SB) is internally connected together with the source (S), so the drain and source are not interchangeable in practice.Their symbols are presented in Fig.11.

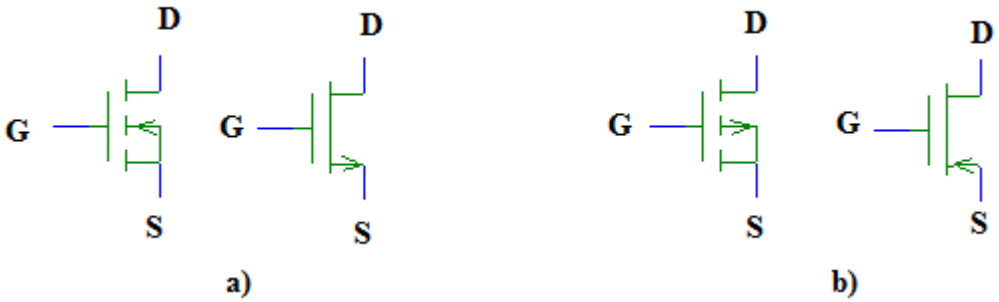


Fig.11.The electrical symbol for the discrete MOSFET transistor:
a) n-channel MOSFET; b) p-channel MOSFET

Current flow in a MOS device is a function of several material, structural, and bias parameters, including (Fig.12): the channel length L, which is the separation distance between the source and drain; the channel width W, charge mobilities within the active channel region (μ_n for electrons or μ_p for holes); the capacitance of the oxide layer C_{ox}, which is modeled as a parallel plate capacitor and is in turn a function of oxide layer thickness (t_{ox}) and permittivity (σ); the gate-source potential V_{GS}; the drain to source bias V_{DS}; and the threshold voltage V_T. The threshold voltage is dependent on the impurity concentration of the channel region. Additionally, since several breakdown mechanisms associated with MOS structures are contingent on the maximum electric field in the drain space charge region, doping criteria may become important to reduce these effects.

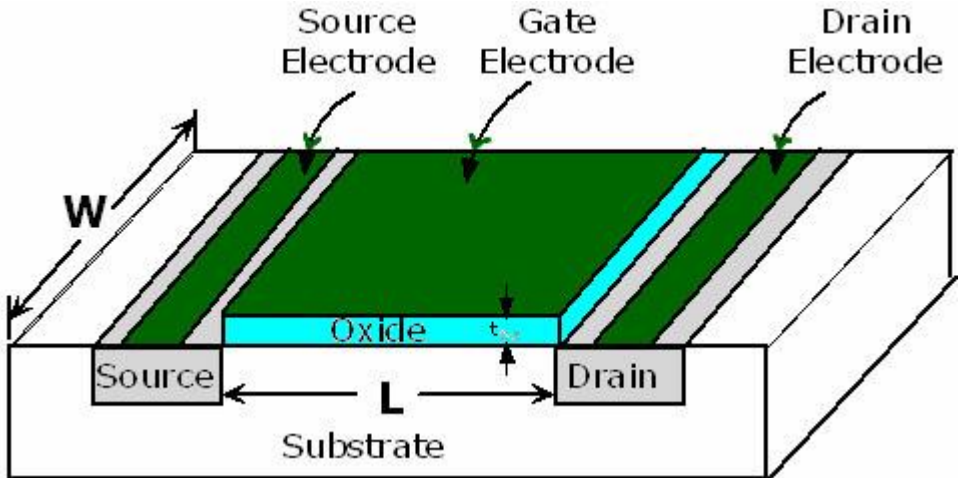


Fig.12.The mechanical parameters for the MOSFET transistor

Due to the insulator layer that exists between the gate and the substrate (SiO_2), we can modify the device structure to allow two modes:

- In the **depletion mode**, a channel region of a material type corresponding to the majority carrier (i.e., n-type material for NMOS and p-type material for PMOS) is physically implanted at the time of fabrication to connect the source and drain. Recall that an active (a.k.a. conduction or inversion) channel is required for current to flow between the source and drain, so the depletion MOSFET is in a normally on condition until the field effect is used to turn it off. To turn a depletion type MOS transistor off, or interrupt current flow between the source and drain, appropriate bias conditions must be generated in order to deplete the channel region of charge carriers, thereby removing the conduction path between source and drain.
- Conversely, in the **enhancement mode**, the conduction channel is created through the field effect. Enhancement mode operation is characterized by the requirement that appropriate biasing conditions be applied to create a conduction channel between the source and drain diffusions. In this mode of operation, the transistor exists in a normally off state until the conduction channel is created and current can flow between the source and drain.

By considering the majority carrier types in the semiconductor (electrons and holes) and two possible modes of operation (depletion mode and enhancement mode) as defined above, the MOSFET device types are: **depletion NMOS transistor, depletion PMOS transistor, enhancement NMOS transistor and enhancement PMOS transistor.**

a. The n-channel depletion MOS transistor

The depletion NMOS device (Fig.13) is formed from a p-type substrate with physically implanted n-type source, drain and channel regions. The dielectric material covers the area between the source and drain to provide electrical isolation as mentioned earlier and allows the field-effect operation to occur. For a gate-to-source voltage (V_{GS}) greater than or equal to zero, the channel is active and, if a sufficiently large drain-to-source voltage (V_{DS}) is applied, electrons will move through the channel from the source to the drain, for a positive drain current ($I_D>0$).

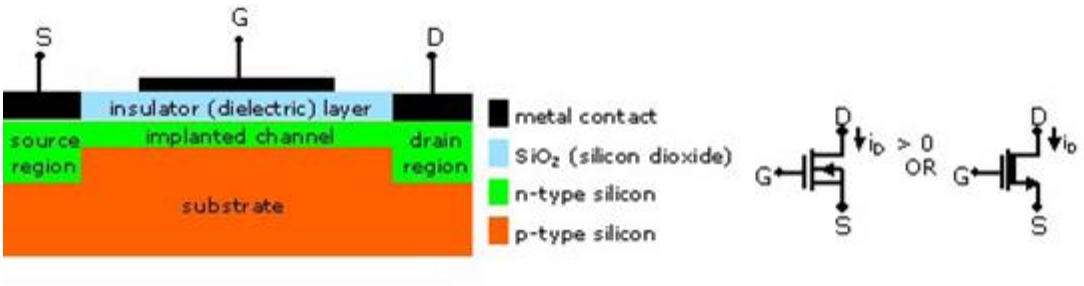


Fig.13.The structure and the symbols of the depletion NMOS transistor

When no DC voltage is applied between the gate and the source ($V_{GS}=0$), the implanted channel will remain unchanged. If the potential between the gate and the source is increased ($V_{GS}>0$), more majority carriers will be attracted to the channel at the Si/SiO_2 interface. Charges cannot move through the insulator (ideally), so a positive applied gate bias has the effect of attracting more negative charges from the substrate to the channel. Note that since the gate is isolated from the source (and the channel) by the oxide layer, the gate current is negligibly small and may be considered to be zero. Now, if we have a conduction channel and apply a large enough positive V_{DS}(remember that this means the potential at the drain is higher than that of the source), electrons in the channel (and source region) will be attracted to the drain. The channel size is increased, resulting in an increased drain current.

For a negative V_{GS}, the potential at the gate is less positive than that of the source. Usually the source is grounded, so this means that the gate potential is negative, or that negative charges are "piled up" along the gate contact. Since like charges repel, the negative charges on the gate push electrons out of the channel region and into the substrate, thereby depleting the majority carriers in the channel when V_{GS} reaches a specific magnitude known as the **threshold voltage** V_T. At this threshold value, the channel is considered to be completely depleted of majority carriers and the drain current magnitude is reduced to zero for any applied V_{DS}.

b. The p-channel depletion MOS transistor

The depletion PMOS device (Fig.14) is complementary to the depletion NMOS except the n-type and p-type silicon designations are interchanged. This device operates exactly as discussed above, with the following modifications:

- The conduction channel exists for $V_{GS} \leq 0$, with the conductivity increasing for negative V_{GS} (more holes are attracted to the channel region. For a negative V_{DS} of sufficient magnitude, current flows through the channel).
- To deplete the channel in a PMOS device, a positive V_{GS} is applied since the positive gate will repel the holes in the channel. The channel is again pinched off at a threshold voltage V_T, but instead of being a negative as for the depletion NMOS, it is now positive with a magnitude that depends on specific material and structural parameters. Above the threshold voltage magnitude, I_D is once again zero regardless of the applied V_{DS}.

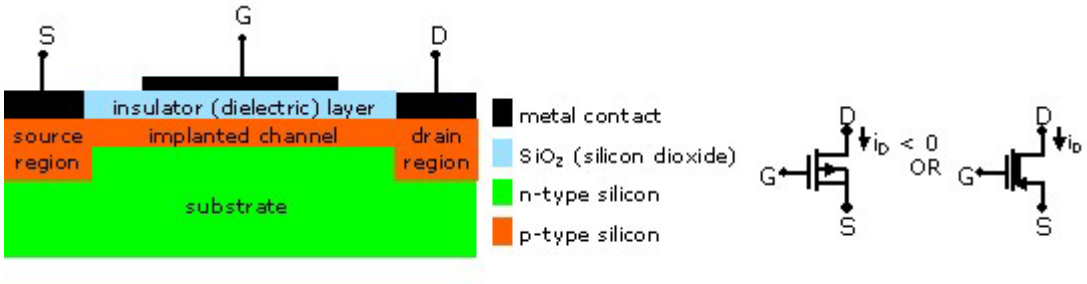


Fig.14.The structure and the symbols of the depletion PMOS transistor

c. The n-channel enhancement MOS transistor

The enhancement NMOS device (Fig.15) differs from the depletion NMOS by the absence of the implanted channel.

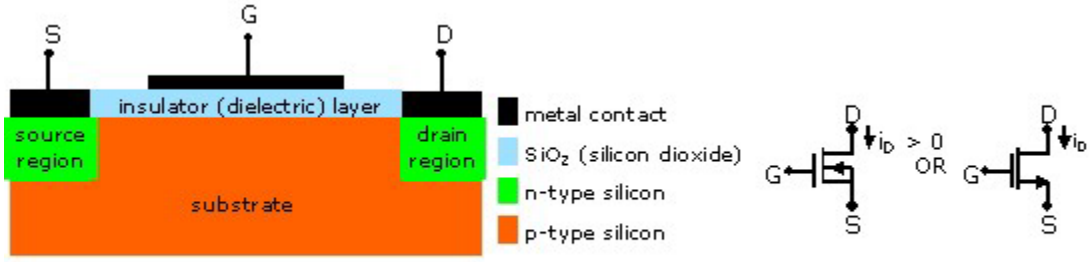


Fig.14.The structure and the symbols of the enhancement NMOS transistor

This type of device is normally off and requires the creation of a conduction channel to allow current to flow. For the NMOS structure, this is achieved by applying a positive V_{GS} of sufficient magnitude ($V_{GS} > V_T$). The positive gate potential attracts electrons from the substrate to the Si/SiO_2 interface under the oxide layer. This process continues until enough electrons have been accumulated between the source and drain to increase the

conductivity to a point that a conduction channel is formed. Note that no appreciable drain current can flow until the V_{GS} magnitude exceeds the threshold voltage V_T.
The remainder of device operation is as discussed for the depletion NMOS. Once the channel has been created, a positive V_{DS} will result in a drain current I_D.

d. The p-channel enhancement MOS transistor

The enhancement PMOS transistor is represented in Fig.16. Because it does not have a built-in channel and holes are the majority carriers, a negative V_{GS} with a magnitude greater than V_T must be applied to create the conduction channel. Once the channel is created and drain current can flow, a negative V_{DS} of appropriate magnitude results in a negative drain current.

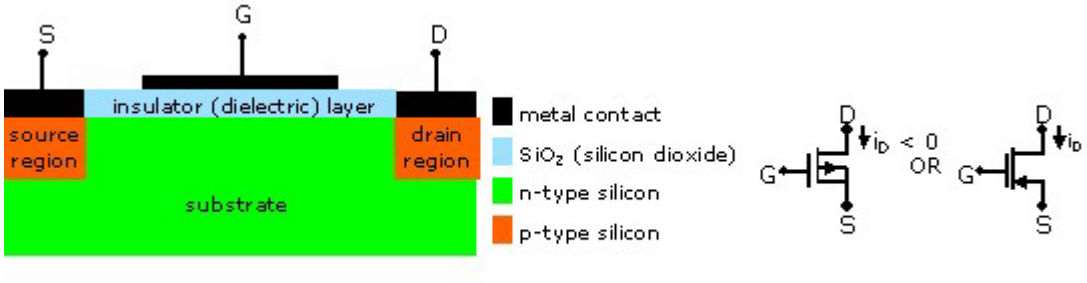


Fig.16.The structure and the symbols of the enhancement PMOS transistor

In Fig.17 are represented the transfer characteristics ($I_D(V_{GS})$) for the depletion and enhancement n type and p type MOSFET transistors.

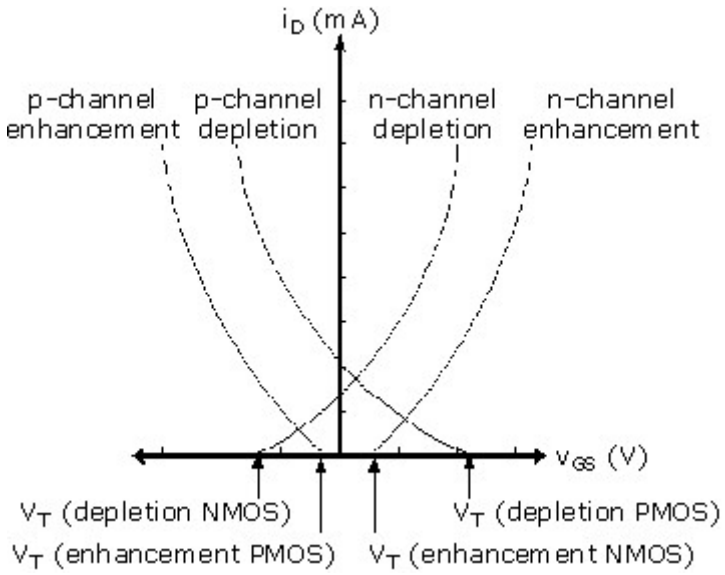


Fig.17.The transfer characteristic for depletion and enhancement MOS transistors

A. Enhancement Mode MOSFET Output Characteristics

The enhancement mode MOSFET devices have the output characteristics presented in Fig.18. The following aspects are taken into account:

- Enhancement mode devices have no built in channel (i.e., the device is normally off).
- A threshold voltage, determined by physical and fabrication parameters, exists for the MOSFET ($V_T > 0$ for NMOS, $V_T < 0$ for PMOS).

- Generally, the source is grounded and is common to both gate and drain.
- An active channel is created between drain and source (the transistor is turned on) through the application of a gate voltage of appropriate polarity and magnitude ($V_{GS} - V_T > 0$ for NMOS, $V_{GS} - V_T < 0$ for PMOS).
- Current flow between the drain and source is a function of both V_{GS} and V_{DS}.

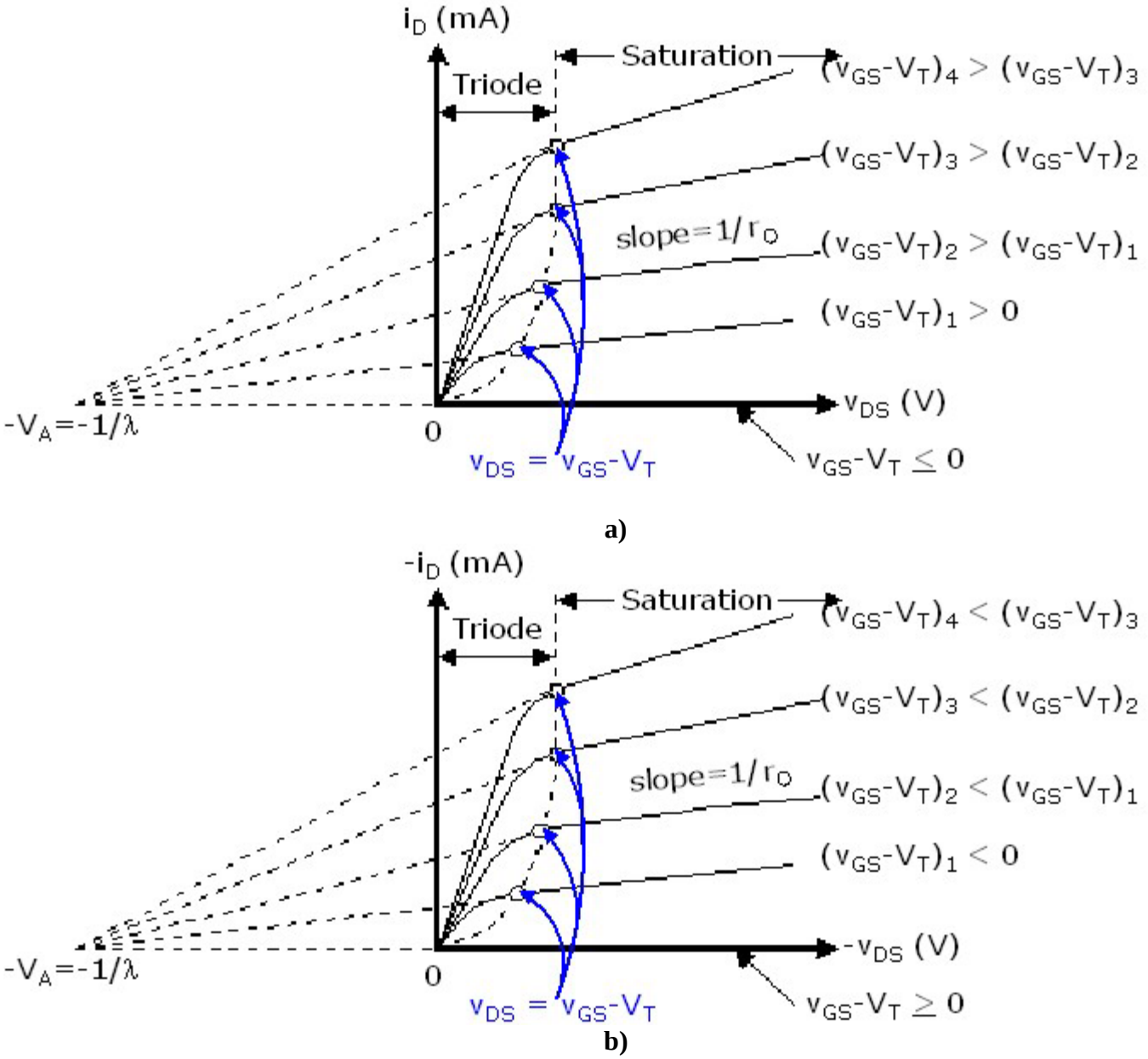


Fig.18.The output characteristic for enhancement MOS transistors: a) N-MOSFET; b) P-MOSFET

Once the device has been turned on ($V_{GS}>V_T$ for NMOS, $V_{GS}<V_T$ for PMOS), current may flow between drain and source with an applied V_{DS}, generating individual curves for different values of V_{GS}-V_T. The MOSFET has different operational regions, depending upon external biases. The delineation of the two regions for the MOSFET (triode and saturation) is determined by the relationship between the applied drain-to-source voltage, the applied gate-to-source voltage and the threshold voltage, which occurs when $V_{DS}= V_{GS}-V_T$.

If $|V_{DS}|< |V_{GS}-V_T|$, the transistor is operating in the **triode** region and the relationship between I_D and V_{GS} is approximately linear. This allows the MOSFET to be operated as a linear resistor whose resistance is controlled by V_{GS}. In the triode region, the potentials at all three terminals strongly affect the drain current, and the drain current obeys the relationship:

$$I_{Dn} = K_n \cdot \left[2 \cdot \left(V_{GS} - V_T \right) \cdot V_{DS} - V_{DS}^2 \right] \tag{5}$$

$$K_n = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \tag{6}$$

$$I_{Dp} = K_p \cdot \left[-2 \cdot \left(V_{GS} - V_T \right) \cdot V_{DS} - V_{DS}^2 \right] (\textit{positive} \text{ value}) \tag{7}$$

$$K_p = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} \tag{8}$$

If V_{GS} is kept constant and the $|V_{DS}|$ is increased, voltage in the channel varies from zero (when measured at the source) to V_{DS} (when measured at the drain). Now, if we simultaneously consider the effect of V_{GS}, we can see that both sources are trying to attract charges (electrons for the n-MOSFET, holes for the p-MOSFET) and they are essentially opposing each other. Since the gate-to-source voltage controls the channel depth, and V_{GS} and V_{DS} are essentially competing for available charges, the channel does not have a uniform depth for any V_{DS}. In fact, the effective gate-to-source voltage decreases from the applied $|V_{GS}|$ at the source, to $|V_{GS}-V_{DS}|$ at the drain and the channel takes on a tapered shape.
Another way of looking at this effect is to consider the gate-to-drain voltage V_{GD}:

$$V_{GD} = V_G - V_D = \left(V_G - V_S \right) - \left(V_D - V_S \right) = V_{GS} - V_{DS} \tag{9}$$

When $V_{GS} - V_{DS} \geq V_T$ for n-channel MOSFET or $V_{GS} - V_{DS} \leq V_T$ for p-channel MOSFET, the depth of the active channel becomes zero and the channel is constrained or pinched off. This means that further increases in $|V_{DS}|$ have little effect on I_D (ideally, no effect).
For $|V_{DS}|>|V_{GS}-V_T|$ the transistor is in the normal active, or saturation region of operation, with the boundary between the triode and saturation regions (called the **knee**) defined by $V_{DS}=V_{GS}-V_T$. If we could have an ideal device, the curves in the saturation region would be perfectly horizontal. The expression for the drain current of an ideal MOSFET in saturation is:

$$I_D = K \cdot \left(V_{GS} - V_T \right)^2 \cdot \left(1 + \lambda \cdot V_{DS} \right) \tag{10}$$

,where λ is the channel length modulation parameter. Often, the term $|\lambda \cdot V_{DS}| << 1$, so the expression becomes:

$$I_D = K \cdot \left(V_{GS} - V_T \right)^2 \tag{11}$$

The output resistance of the device (r_O) is:

$$r_O = \left[\frac{\partial v_{DS}}{\partial i_D} \right] \tag{12}$$

$$r_O = \frac{1}{K \left(V_{GS} - V_T \right)^2 \cdot \lambda} \approx \frac{1}{\lambda \cdot I_D} = \frac{V_A}{I_D} \tag{13}$$

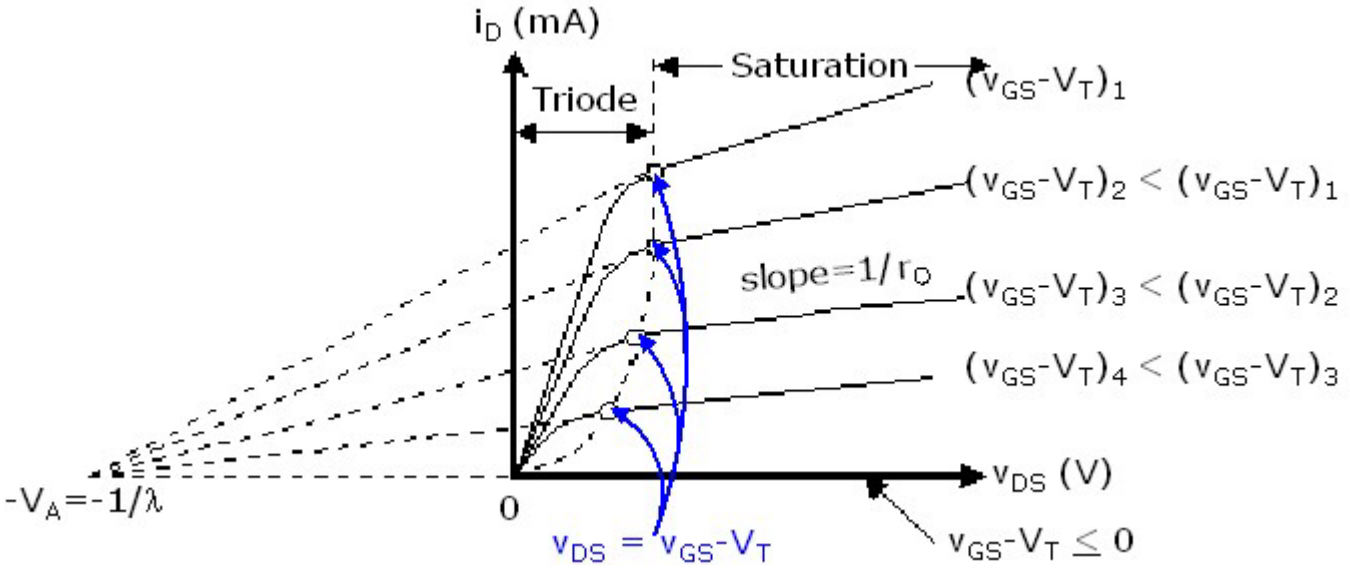
A. Depletion Mode MOSFET Output Characteristics

In the depletion mode, the device has the following characteristics:

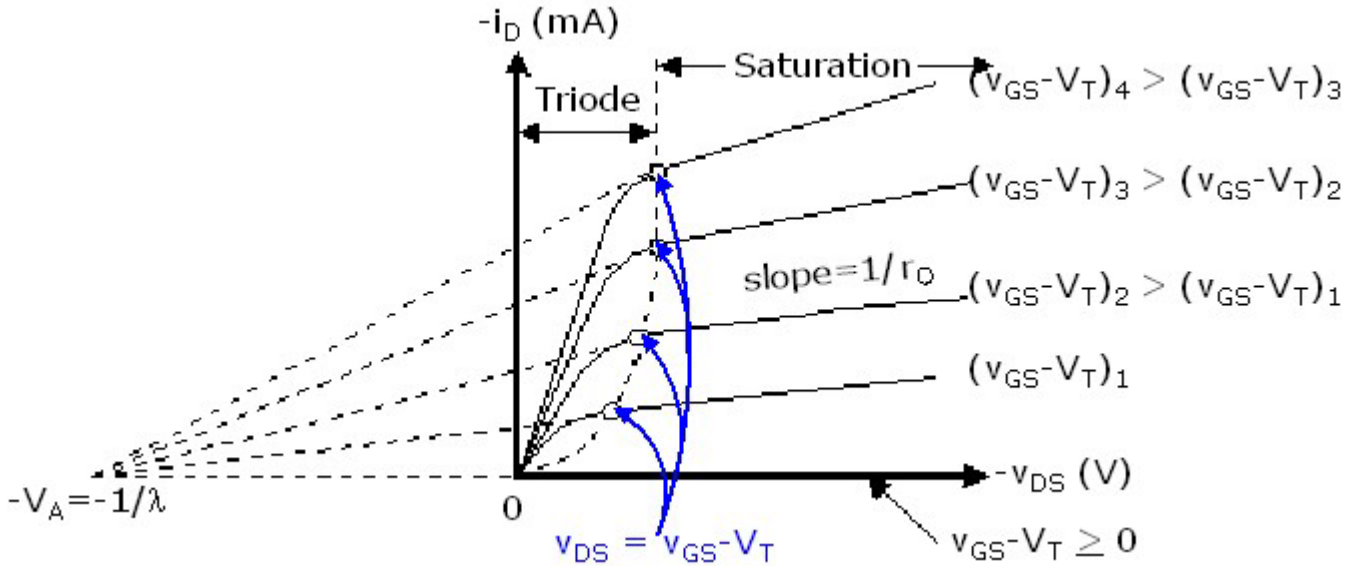
- Depletion mode devices have a built in channel (the device is normally on).
- A threshold voltage, determined by physical and fabrication parameters, exists for the MOSFET ($V_T<0$ for n-channel MOSFET, $V_T>0$ for p-channel MOSFET)
- Generally, the source is grounded and is common to both gate and drain.

- The active channel is depleted between drain and source (the transistor is turned off) through the application of a gate voltage of appropriate polarity and magnitude (V_{GS}-$V_T \leq 0$ for n-channel MOSFET, V_{GS}-$V_T \geq 0$ for p-channel MOSFET).
- Current flow between the drain and source is a function of both V_{GS} and V_{DS}. However, in the depletion mode, current can flow for both positive and negative values of V_{GS} for both NMOS and PMOS devices until the cutoff condition is reached.

In Fig. 19 is presented the output characteristic for depletion MOS transistor.



a)



b)

Fig.19.The output characteristic for depletion MOS transistors: a) N-MOSFET; b) P-MOSFET

The equations for depletion MOS transistors are identical to the equations for the enhancement mode transistors.

The MOSFET small signal AC model at low frequencies

The AC small signal model for low frequencies (below 10KHz) of the MOSFET is given in Fig.20. The transconductance (g_m) and the output resistance of the device (r_o) are:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = 2 \cdot K \cdot (V_{GS} - V_T)(1 + \lambda \cdot V_{DS}) \approx 2 \cdot K \cdot (V_{GS} - V_T) \quad (14)$$

$$r_O = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{K(V_{GS} - V_T)^2 \cdot \lambda} \approx \frac{1}{\lambda \cdot I_D} \quad (15)$$

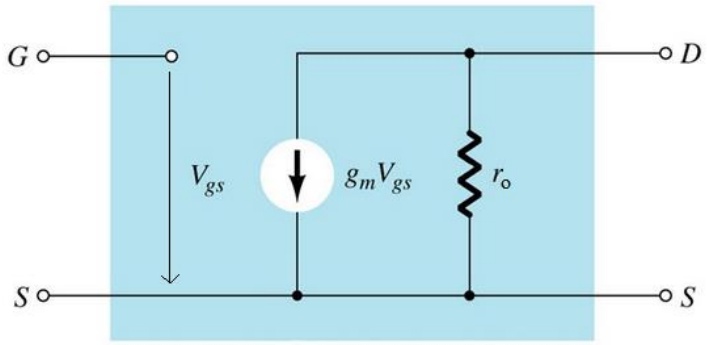


Fig.20.The AC equivalent circuit for MOSFET

3. **Laboratory activity**

a. JFET transfer characteristics

Consider the circuit given in Fig.21. The components are described in *Table 8* from Annex 1. It is required to draw and to simulate the circuit. VGS and VDS are DC voltage supplies.

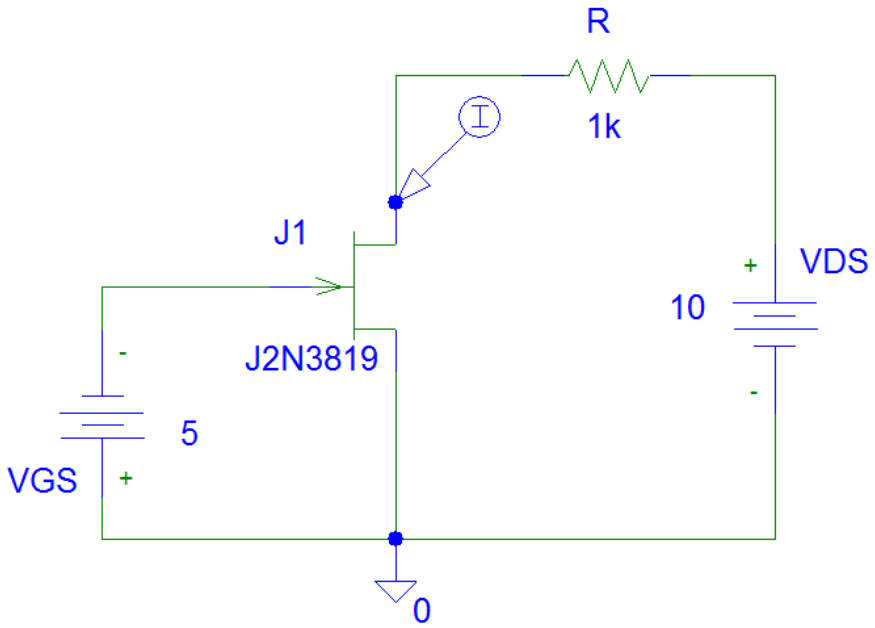


Fig.21 JFET schematic for measuring the transfer characteristics

The drain current (I_D) will be measured as a function of the gate-source voltage (V_{GS}). To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is VGS. It will be varied between 0 and 5V with an increment of 0.1V (Fig.22).

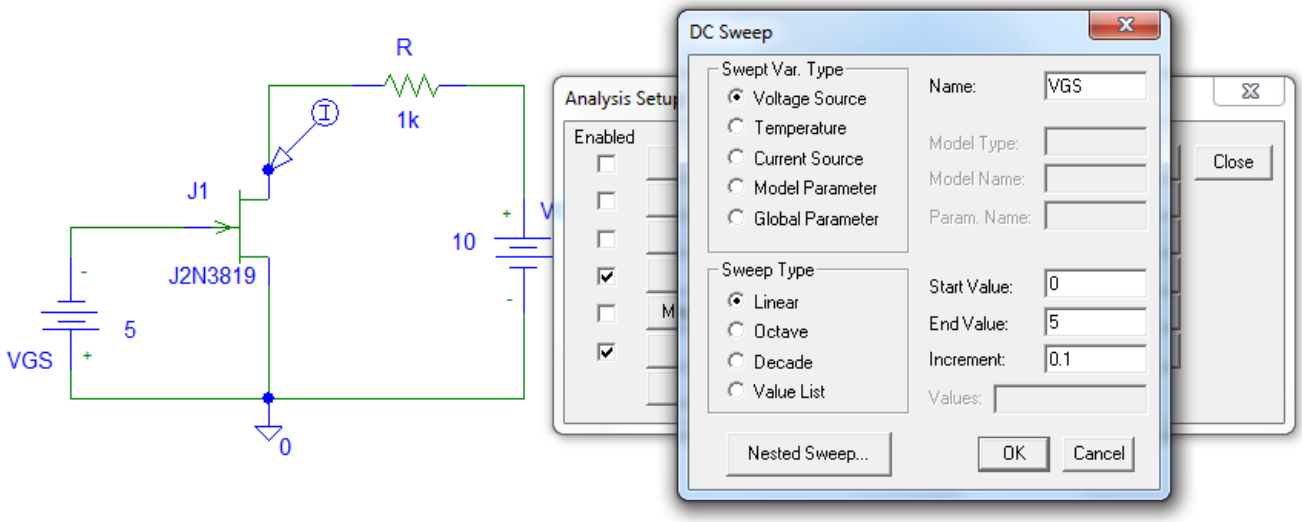


Fig.22 Adjusting VGS for measuring the transfer characteristics

The secondary DC sweep voltage (*Nested Sweep….*) is VDS. It will be varied between 5 and 25V with an increment of 8V. The *Enable Nested Sweep* option will be checked (Fig.23).

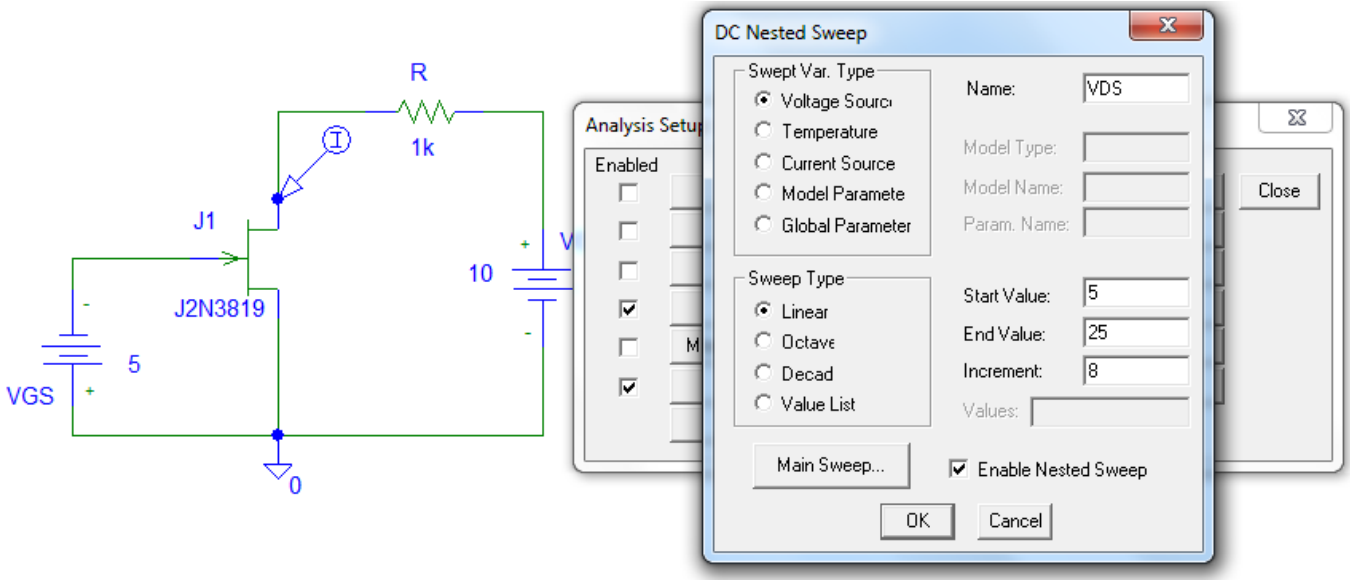


Fig.23 Adjusting VDS for measuring the transfer characteristics

After running the simulation (F11), the drain current will be displayed on Y axis. For the X axis, the selected parameter will be the gate-source voltage which is -V_VGS: *Plot-Axis Settings…-X Axis-Axis Variable….-V_VGS* (Fig.24).

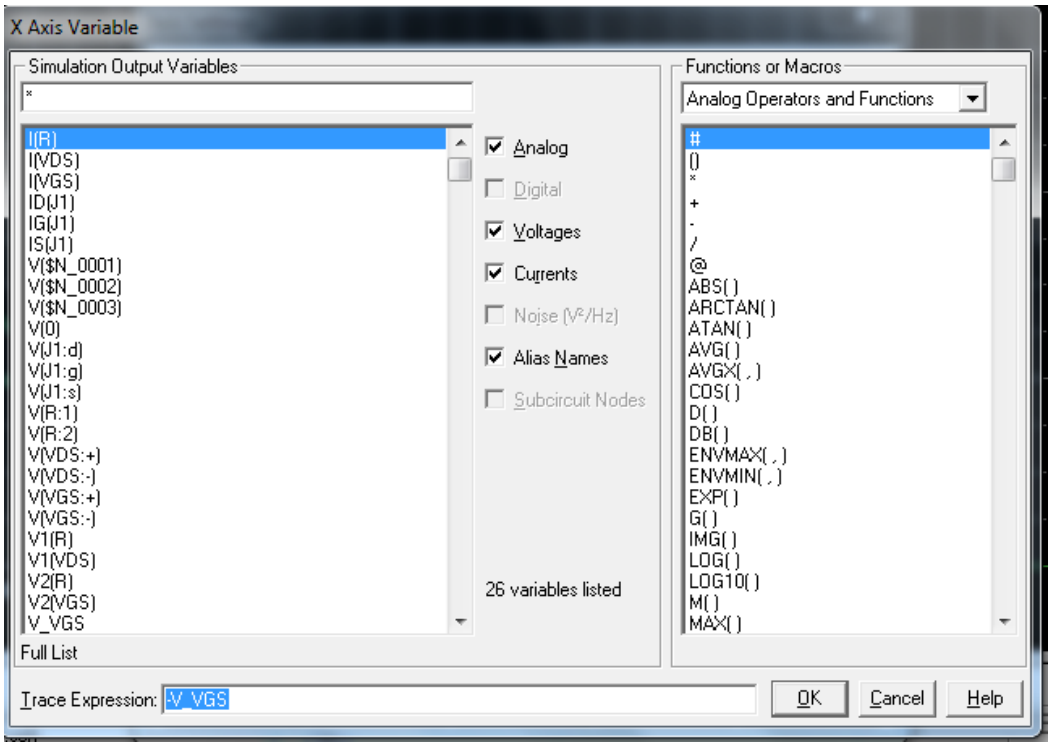


Fig.24 Selecting gate-source voltage on X axis for measuring the transfer characteristics

By selecting the Toggle Cursor, the simulation results may be displayed. For the first two I_D –V_{GS} characteristics, the current saturation occurs because of the drain resistor (R) (Fig.25).

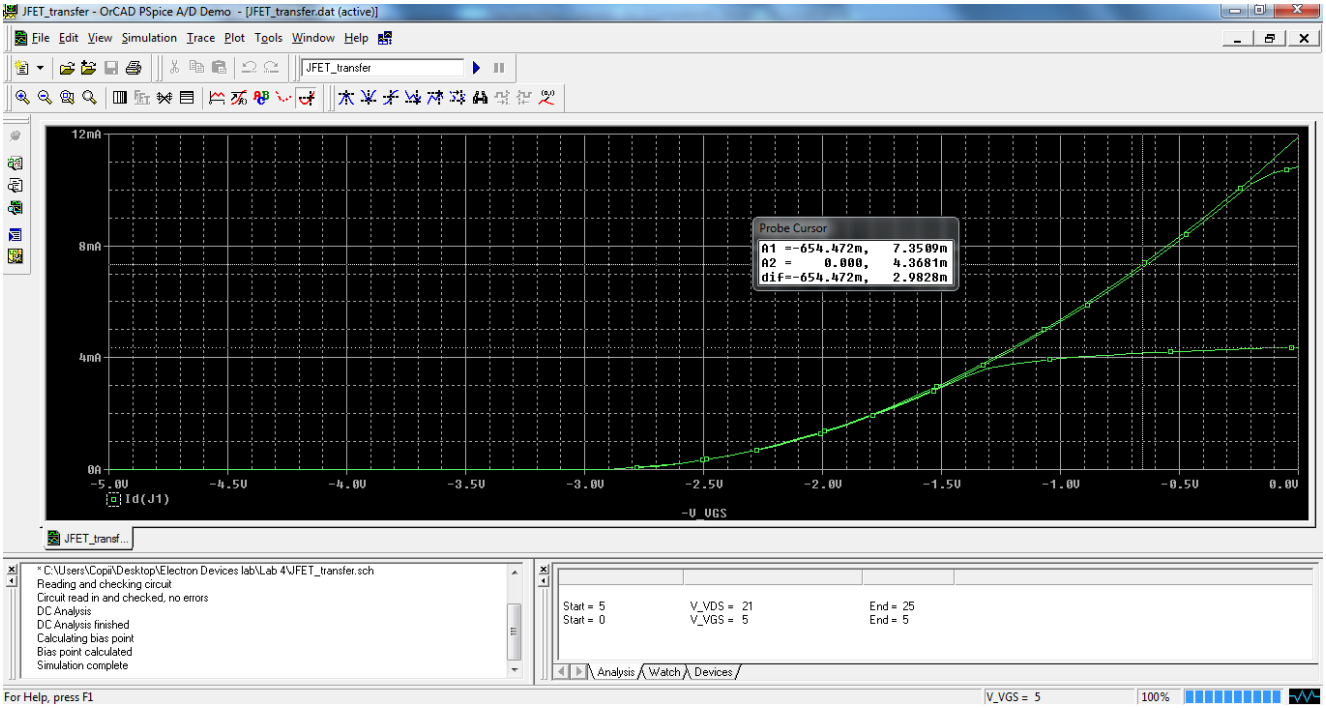


Fig.25. The measurement of the transfer characteristics I_D –V_{GS} for the n-channel JFET

Replace R (1K) by 100 ohms (100) and run the simulation again. Compare the results and complete Table 1.

Table 1 – JFET transfer characteristics

V_{DS}(V)	V_{GS}(V)	I_D(mA)
5	-5	
	-4	
	-2.8	
	-1	
	-0.5	
	0	
13	-5	
	-4	
	-2.8	
	-1	
	-0.5	
	0	
21	-5	
	-4	
	-2.8	
	-1	
	-0.5	
	0	

b. JFET output characteristics

Draw the circuit from Fig.26. It is the same circuit From Fig.21, except some minor changes. VGS and VCC are DC voltage sources.

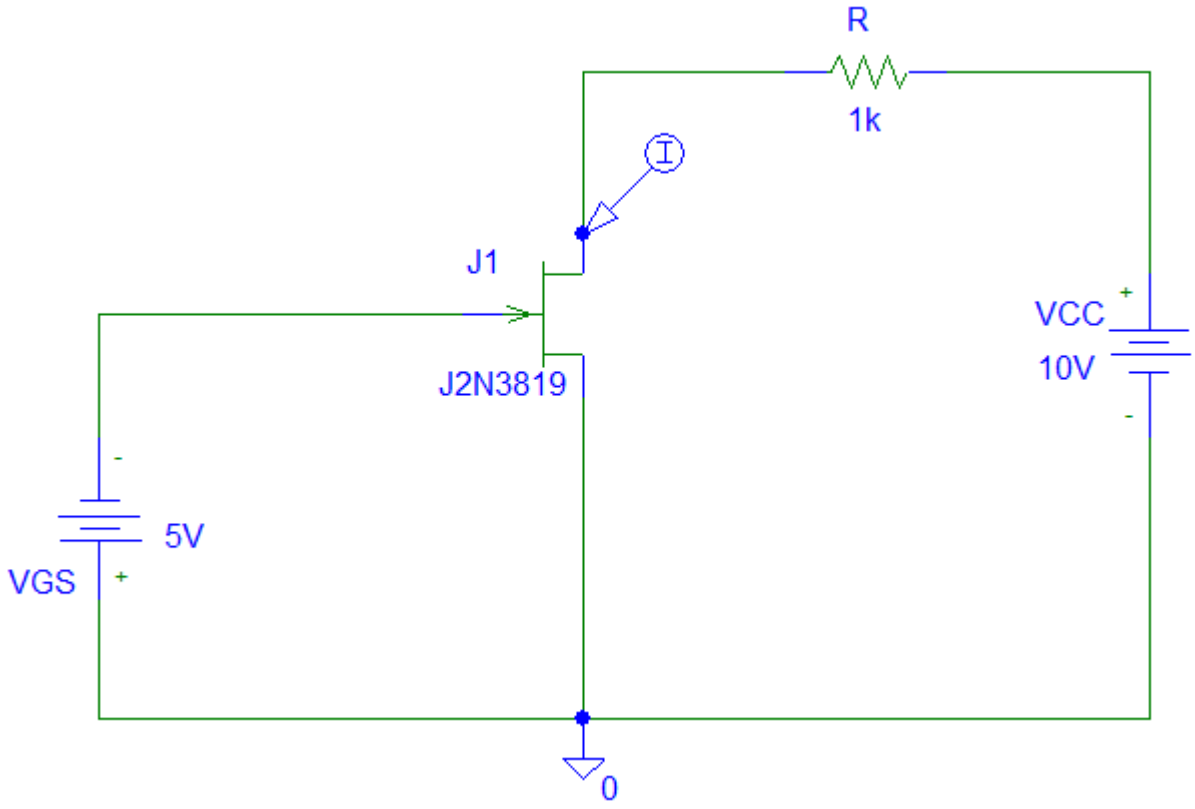


Fig.26 The schematic for measuring the JFET output characteristics

The drain current (I_D) will be measured as a function of the drain-source voltage (V_{DS}). To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is VCC. It will be varied between 0 and 25V with an increment of 1V (Fig.27).

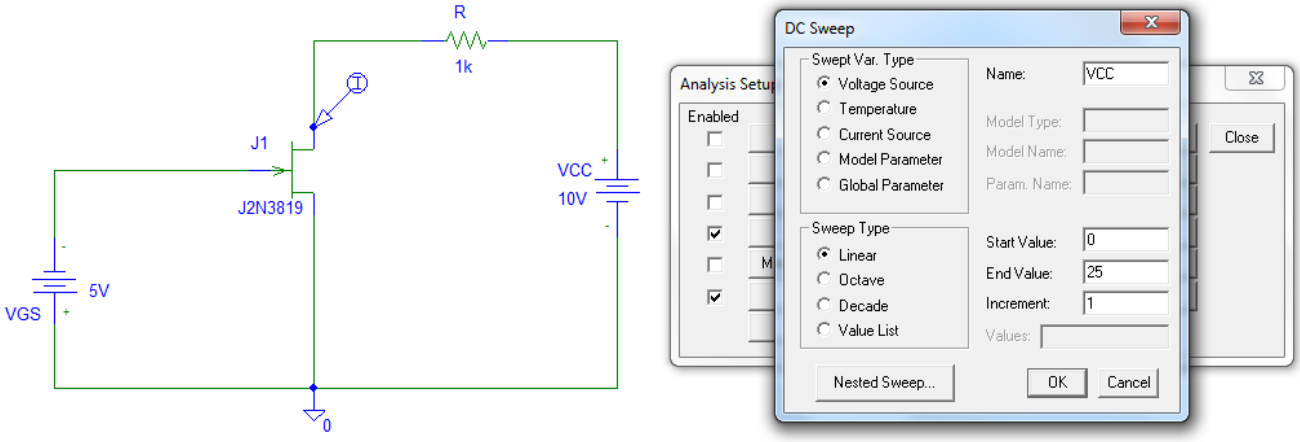


Fig.27 Adjusting VCC for measuring the output characteristics

The secondary DC sweep voltage (*Nested Sweep….*) is VGS. It will be varied between 0 and 3V with an increment of 1V. The *Enable Nested Sweep* option will be checked (Fig.28).

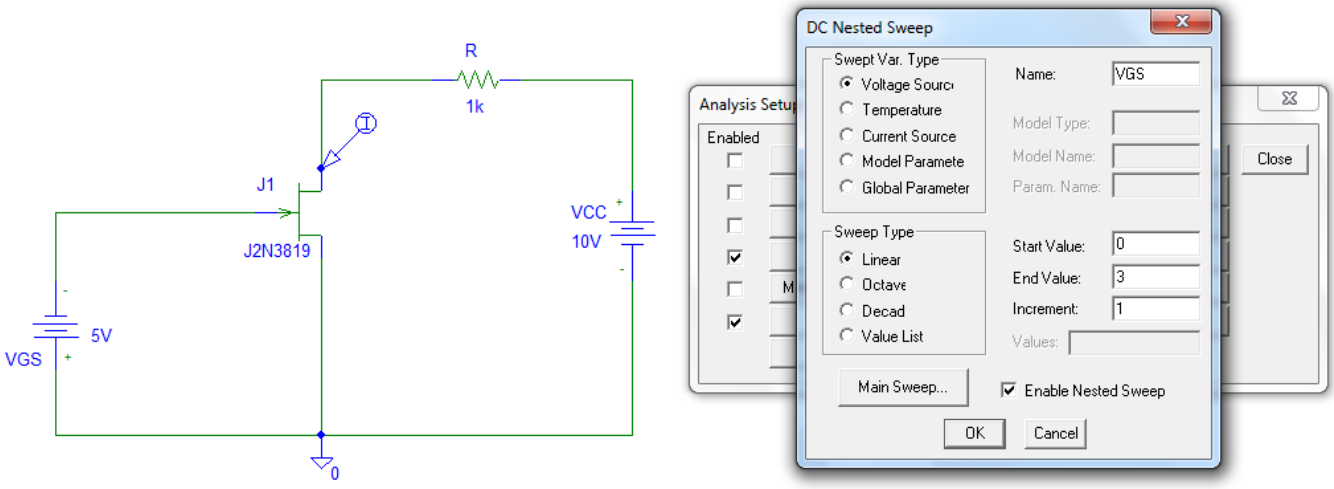


Fig.28 Adjusting VGS for measuring the output characteristics

Then, the simulation may be run (F11). The results are displayed in Fig.29.

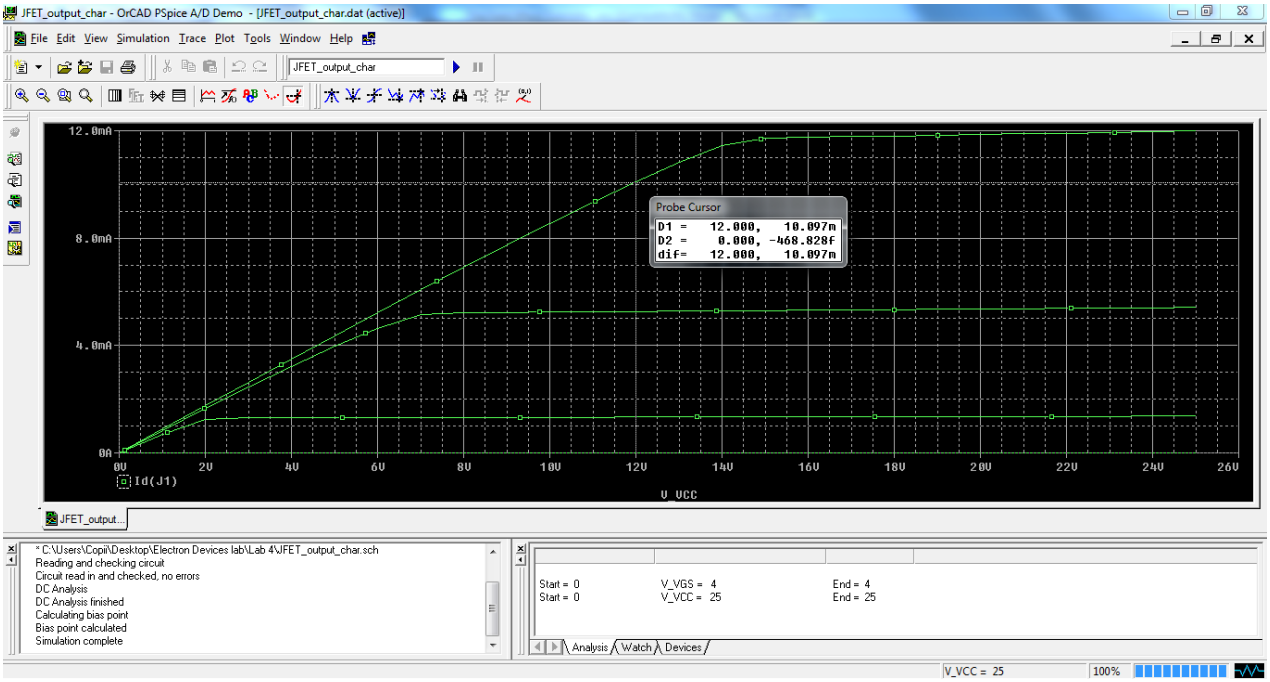


Fig.29. The output characteristics for the n-channel JFET

The simulation results should be written in *Table 2*.

Table 2 – JFET output characteristics

V_{GS}(V)	V_{DS}(V)	I_D(mA)
0	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	20	
	24	
1	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	18	
	20	
	24	

2	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	18	
	20	
	24	
3	0	
	2	
	4	
	6	
	8	
	10	
	12	
	14	
	16	
	18	
	20	
	24	

c. MOSFET transfer characteristics

Look at the circuit from Fig.30. The components are described in *Table 8* from Annex 1. It is required to draw and to simulate the circuit. VGS and VCC are DC voltage supplies.

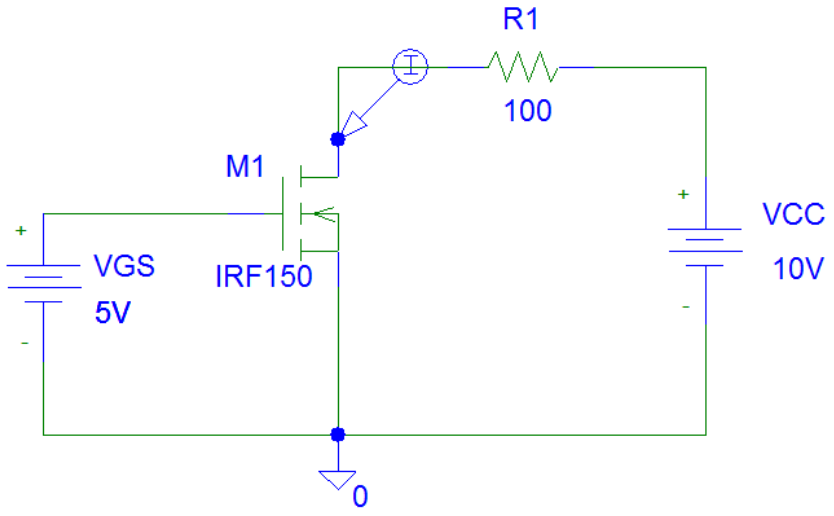


Fig.30. MOSFET schematic for measuring the transfer characteristics

The drain current (I_D) will be measured as a function of the gate-source voltage (V_{GS}). To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is VGS. It will be varied between 2 and 4V with an increment of 0.1V (Fig.31).

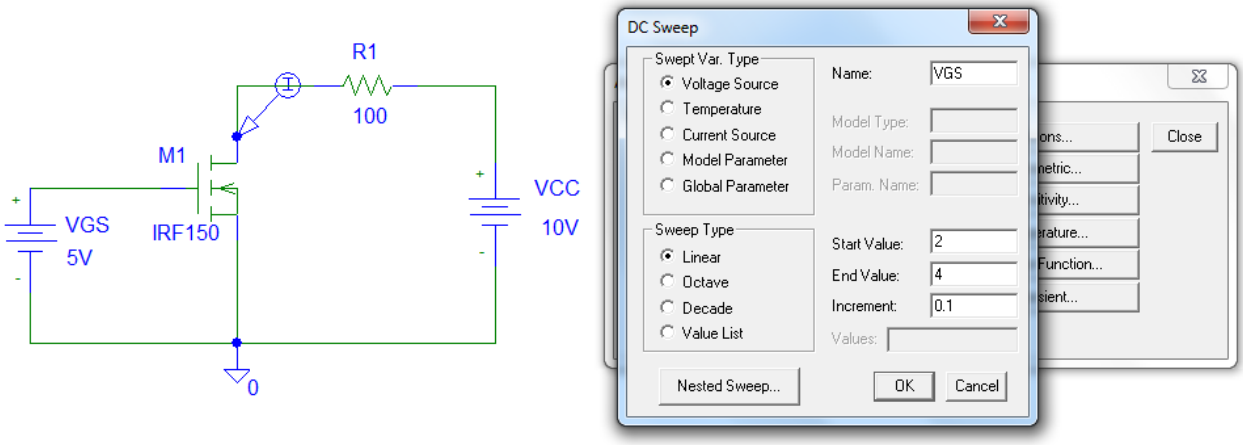


Fig.31. Adjusting VGS for measuring the transfer characteristics

The secondary DC sweep voltage (*Nested Sweep*….) is VCC. It will be varied between 1 and 26V with an increment of 5V. The *Enable Nested Sweep* option will be checked (Fig.32).

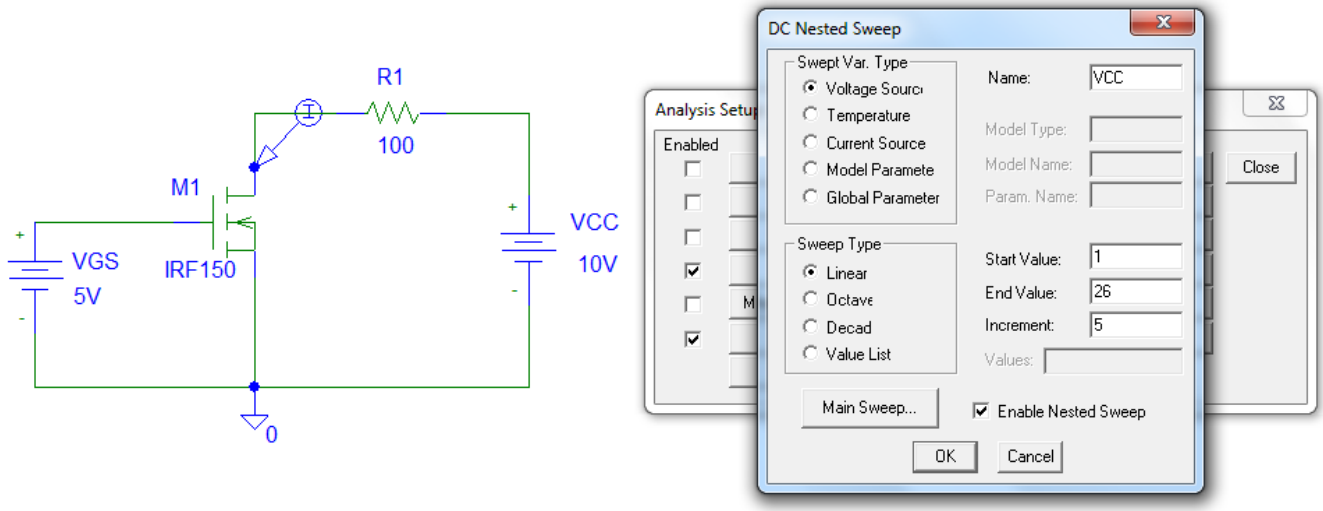


Fig.32. Adjusting VCC for measuring the transfer characteristics

The simulation results (Fig.33) are noted in *Table 3*.

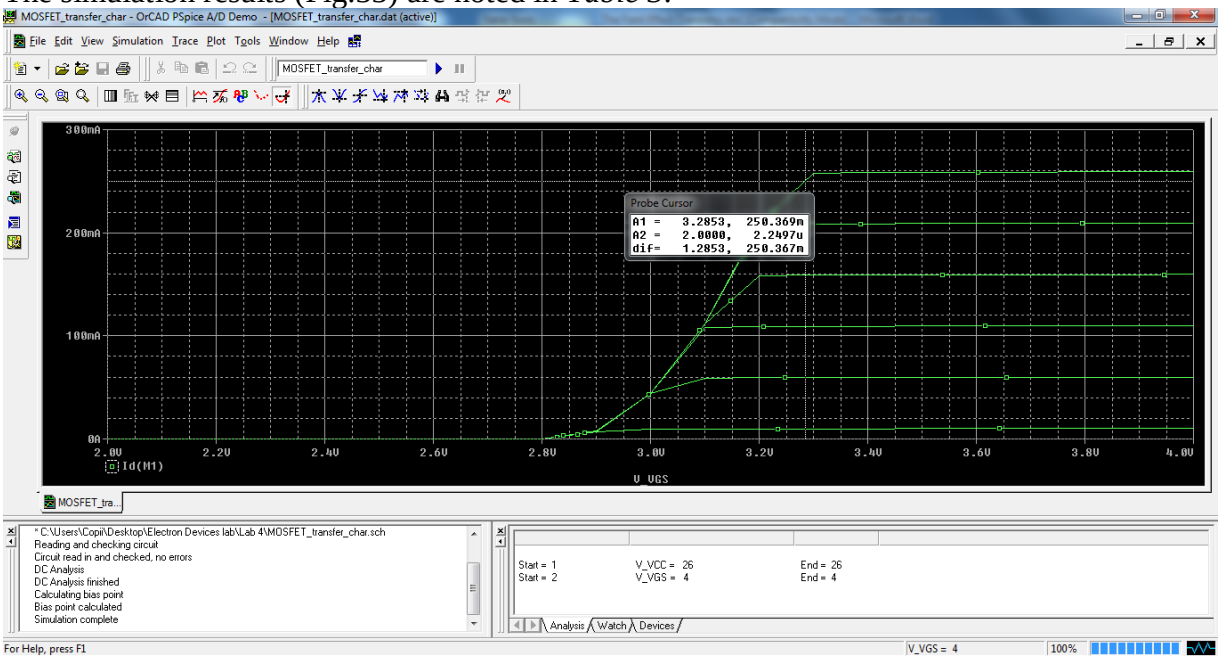


Fig.33.The n-channel MOSFET transfer characteristics

Table 3 – MOSFET transfer characteristics

V_{cc}(V)	V_{GS}(V)	I_D(mA)
1	2	
	2.8	
	2.9	
	3	
	3.1	
	3.2	
	3.3	
	3.4	
	4	
6	2	
	2.8	
	2.9	
	3	
	3.1	
	3.2	
	3.3	
	3.4	
	4	
11	2	
	2.8	
	2.9	
	3	
	3.1	
	3.2	
	3.3	
	3.4	
	4	
16	2	
	2.8	
	2.9	
	3	
	3.1	
	3.2	
	3.3	
	3.4	
	4	
21	2	
	2.8	
	2.9	
	3	
	3.1	
	3.2	
	3.3	
	3.4	
	4	

d. MOSFET output characteristics

Draw the circuit from Fig.34. M1 is an n-channel enhancement MOSFET transistor.

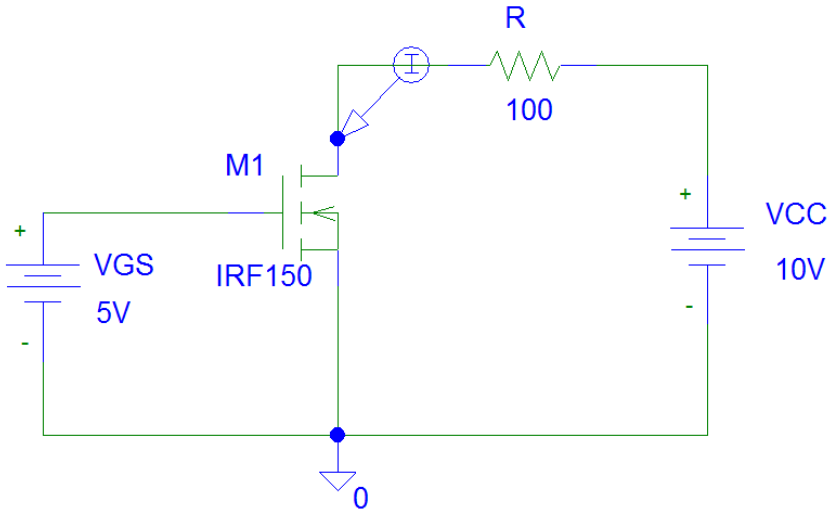


Fig.34.The n-channel MOSFET schematic to measure the output characteristics

A DC sweep simulation will be performed. VCC is the primary sweep voltage with a start value of 0V, end value of 30V, and an increment of 1V.

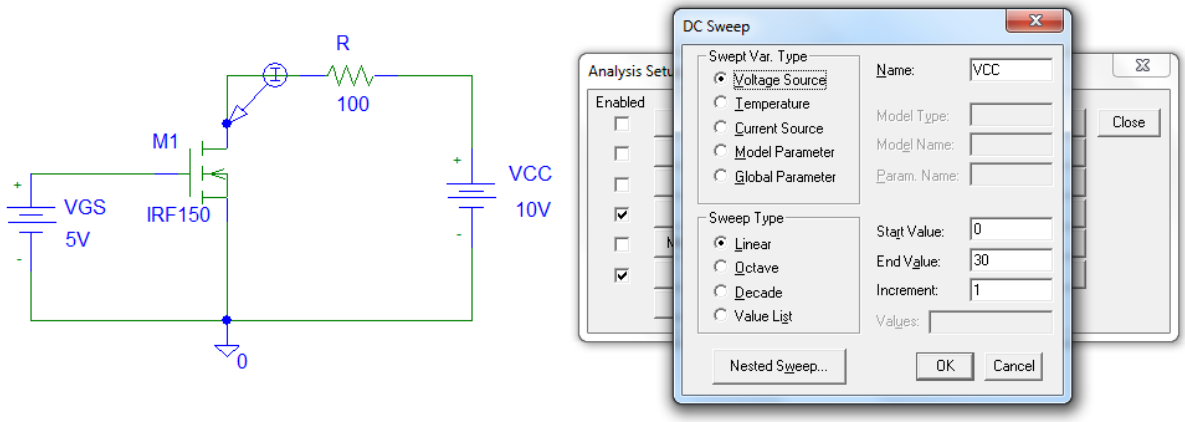


Fig.35.The VCC settings to measure the output characteristics

VGS is the secondary sweep voltage with a start value of 2V, end value of 4V, and an increment of 1V (Fig.36).

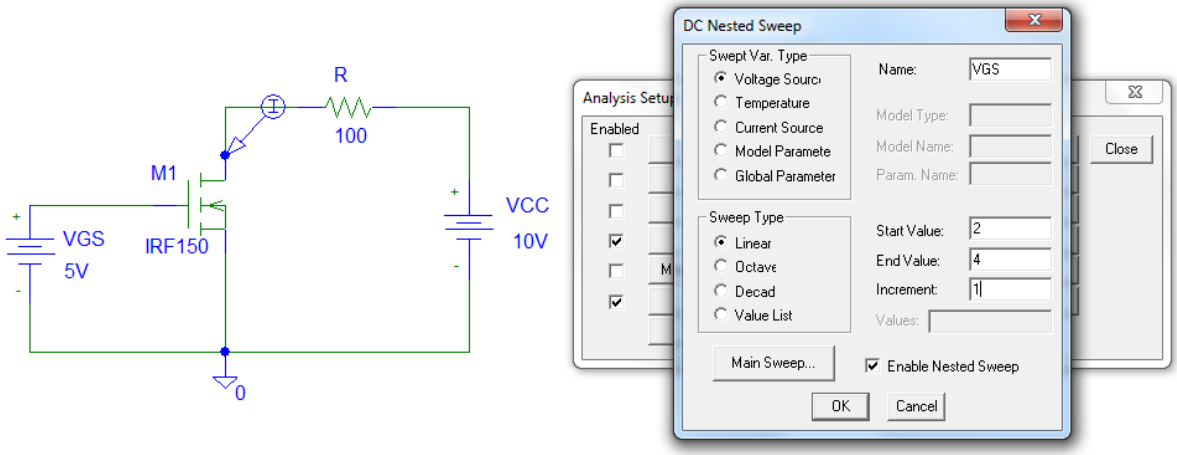


Fig.36.The VGS settings to measure the output characteristics

The simulation results (Fig.37) will be written in *Table 4*.

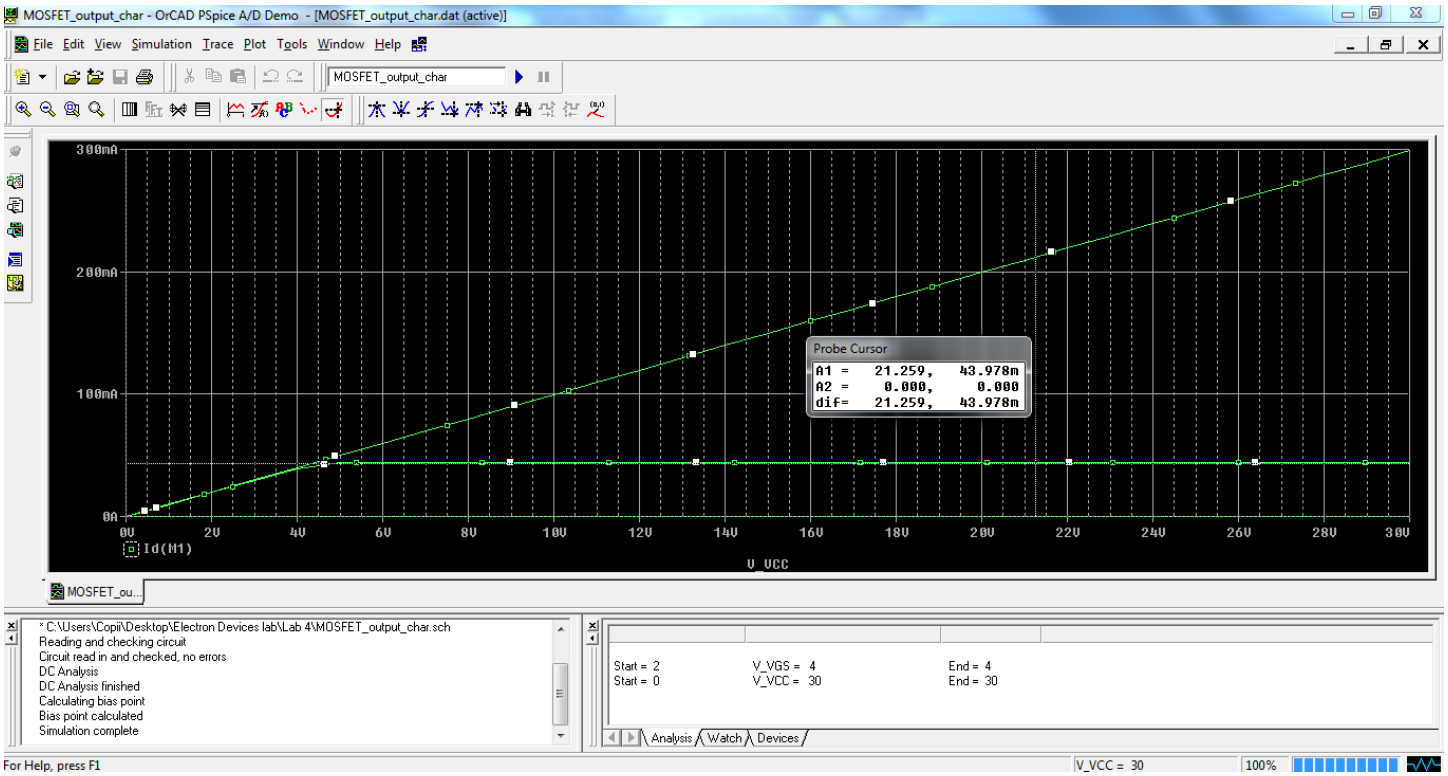


Fig.37.The simulation of the output characteristics for the MOSFET transistor

Table 4 – MOSFET output characteristics

V_{GS}(V)	V_{DS}(V)	I_D(mA)
2	0	
	2	
	4	
	6	
	8	
	10	
	14	
	18	
	22	
	26	
	30	
3	0	
	2	
	4	
	6	
	8	
	10	
	14	
	18	
	22	
	26	
	30	

4	0	
	2	
	4	
	6	
	8	
	10	
	14	
	18	
	22	
	26	
	30	

e. MOSFET current source

Draw the circuit from Fig. 38.

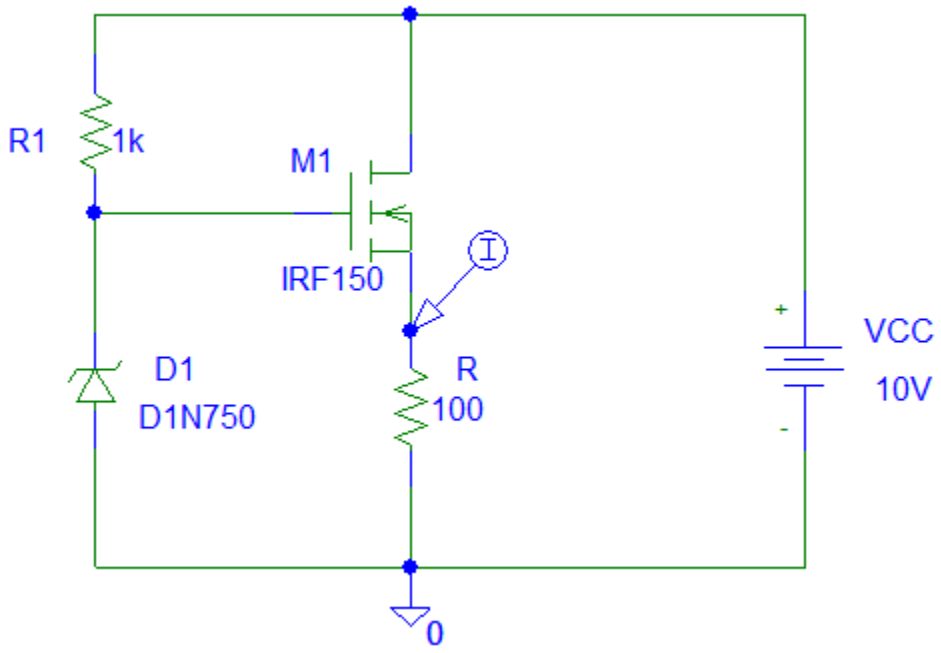


Fig.38. A current source circuit with n-MOS transistor

A DC sweep simulation should be performed. VCC has the parameters: Start Value =10V, End Value =30V, Increment =1.

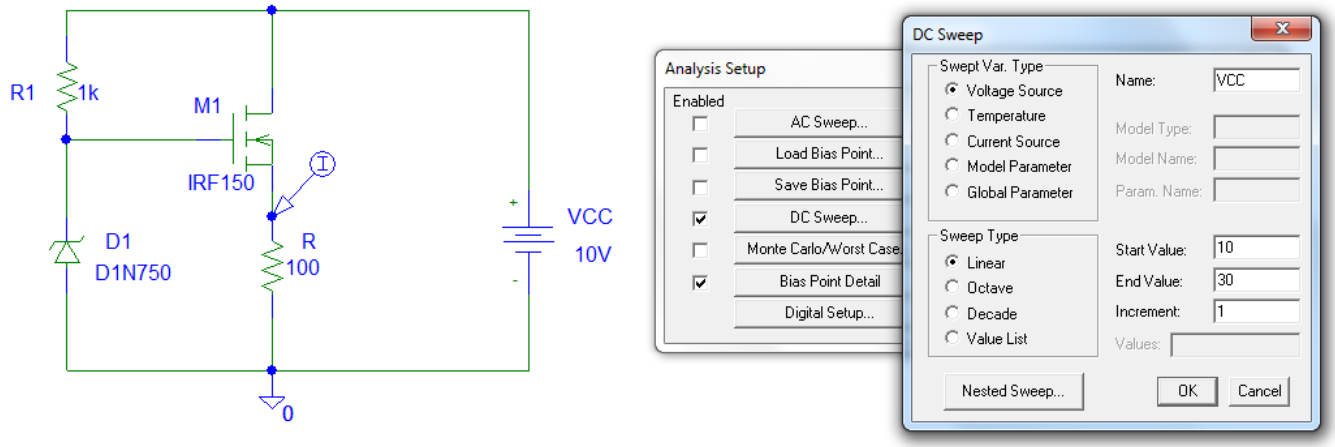


Fig.39. The DC sweep parameters for VCC

The results (Fig.40) should be depicted in *Table 5*.

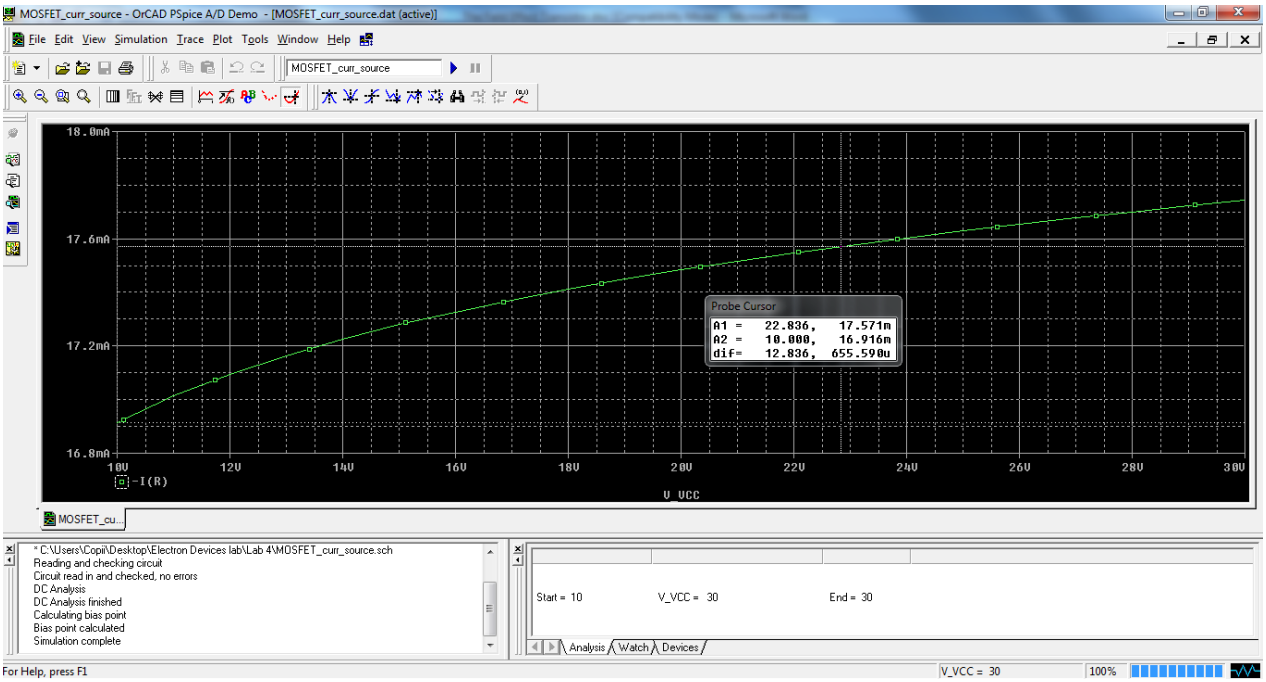


Fig.40.The simulation results for the current source with n-MOS

For the measuring of VDS, you may select: *V(M1:d) - V(M1:s)* in the probe window (*Orcad PSpice A/D demo*).

Table 5

V_G (V)	V_{CC} (V)	V_{DS}(V) =V_{CC}-V_S	I_D(mA)
4.627	10	8.3	16.91
	12		
	14		
	16		
	18		
	20		
	22		
	24		
	26		
	28		
4.712	30		

f. JFET AC amplifier

Consider the small signal AC amplifier which uses a n-channel JFET in the common source configuration (Fig.41). The gate bias is made by 2 voltage sources connected in series: a negative DC voltage source (V_{GS}) with a value of -1V and a sine-wave voltage source (Vac), VSIN, with the parameters: VOFF =0, VAMPL=10mV, FREQ=1k, TD=0, DF=0, PHASE=0.

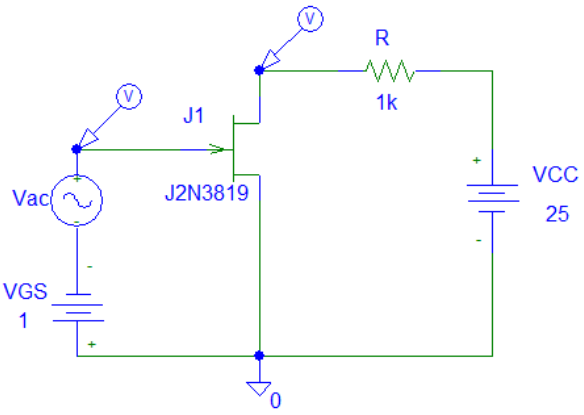


Fig.40.A small signal AC amplifier with n-channel JFET

The simulation should be performed in the time domain (*Transient*), for a time of about 10ms.

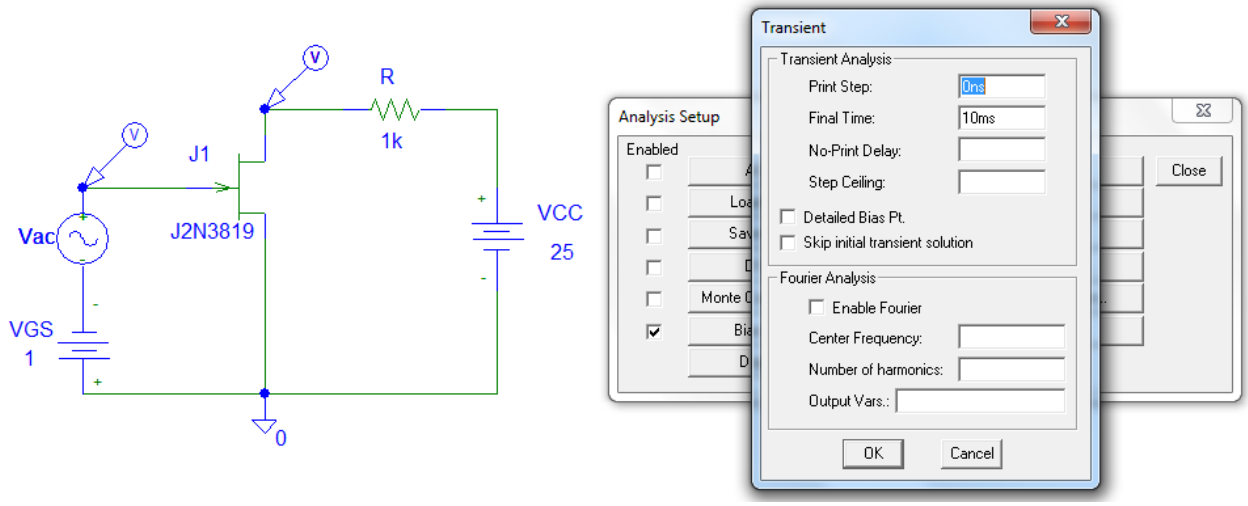


Fig.41. Selecting the Transient simulation for the small signal AC amplifier with n-channel JFET

The output signal may be viewed in the *Probe window*: *OrCAD PSpice A/D Demo* (Fig.42).

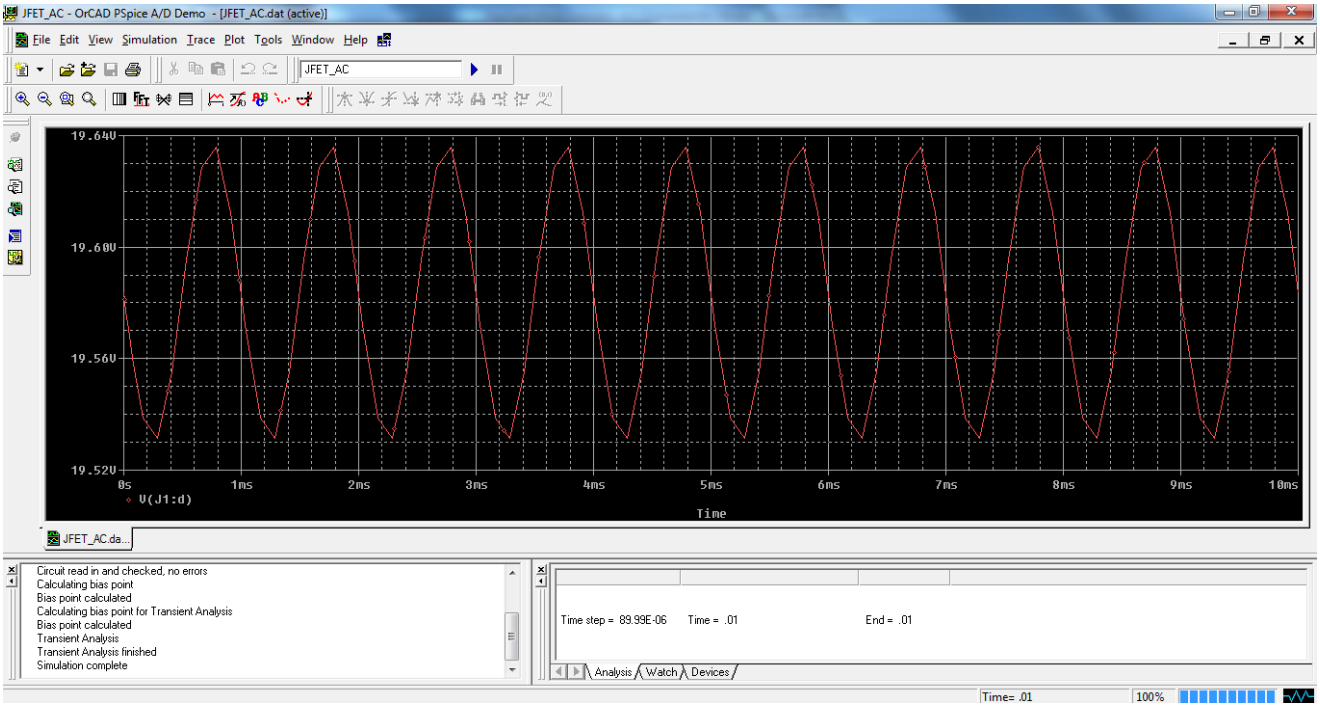


Fig.42.The output signal for the AC amplifier with n-channel JFET transistor

The RMS values for the input (gate) and output (drain) amplitudes may be monitored by selecting: *(MAX(V(J1:g))- MIN(V(J1:g)))/(2*SQRT(2))* for the gate terminal and:
*(MAX(V(J1:d))- MIN(V(J1:d)))/(2*SQRT(2))* for the drain terminal (Fig.43).

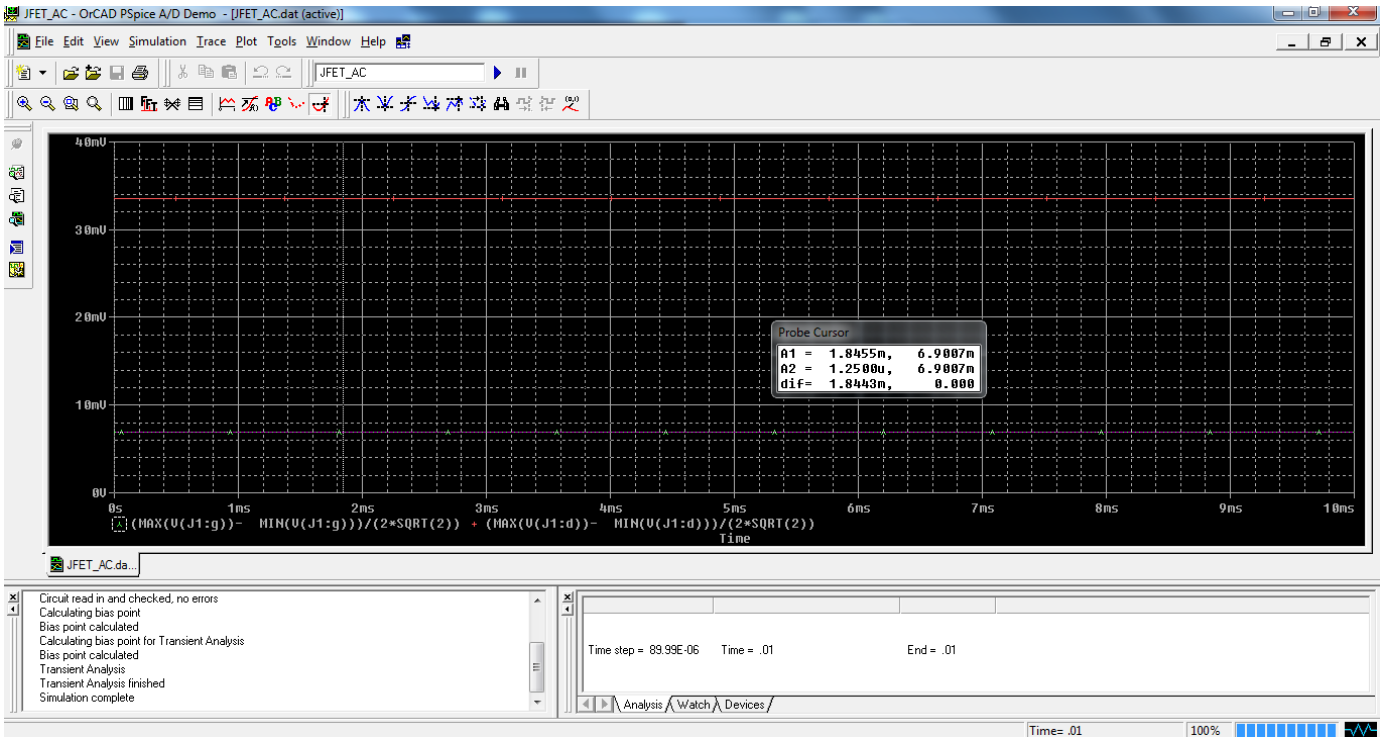


Fig.43.The simulation of the small signal AC amplifier with n-channel JFET transistor (RMS values)

The voltage AC gain is:

$$A_v = \frac{\underline{V_o}}{\underline{V_i}} = \frac{\underline{V_d}}{\underline{V_g}} \tag{16}$$

The current gain is:

$$A_i = \frac{\underline{I_o}}{\underline{I_i}} = \frac{\underline{I_d}}{\underline{I_g}} \tag{17}$$

The transimpedance gain is:

$$A_Z = \frac{\underline{V_o}}{\underline{I_i}} = \frac{\underline{V_d}}{\underline{I_g}} \tag{18}$$

The transadmitance gain is:

$$A_Y = \frac{\underline{I_o}}{\underline{V_i}} = \frac{\underline{I_d}}{\underline{V_g}} \tag{19}$$

Measure the voltages and calculate the AC gains for the amplifier. Compare the phase between the signals. The results should be depicted in *Table 6*.

Table 6

RMS values	A_V	A_I	$A_Z(k\Omega)$	$A_Y(k\Omega^{-1})$
$V_g(mV)$=				
$V_d(mV)$ =				
$I_g(mA)$ =				
$I_d(mA)$ =				

g. MOSFET AC amplifier

Consider the small signal AC amplifier which uses a n-channel MOSFET in the common source configuration (Fig.44). The gate bias is made by 2 voltage sources connected in series: a positive DC voltage source (V_{GS}) with a value of 2.9V and a sine-wave voltage source (Vac), VSIN, with the parameters: VOFF =0, VAMPL=10mV, FREQ=1k, TD=0, DF=0, PHASE=0.

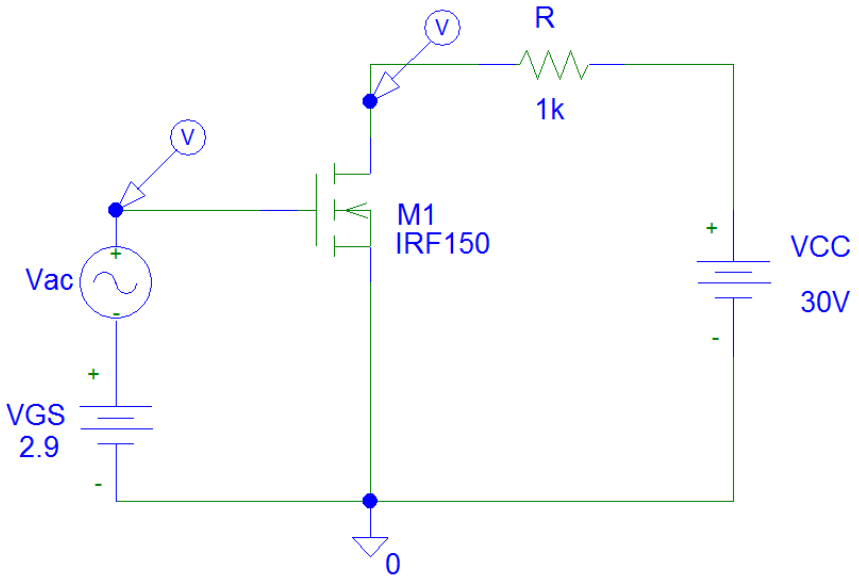


Fig.44.The schematic of the small signal AC amplifier with n-channel MOSFET

The simulation is accomplished in the time domain (*Transient Analysis*).

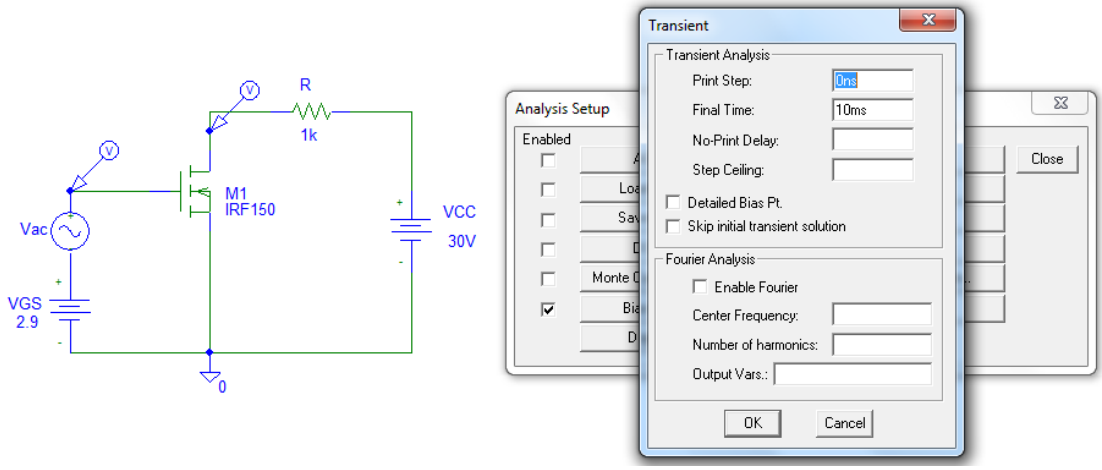


Fig.45.Setting the time domain analysis for the small signal AC amplifier with n-channel MOSFET

Then, the input and the output voltages may be displayed in the *Probe* window (Fig.46).

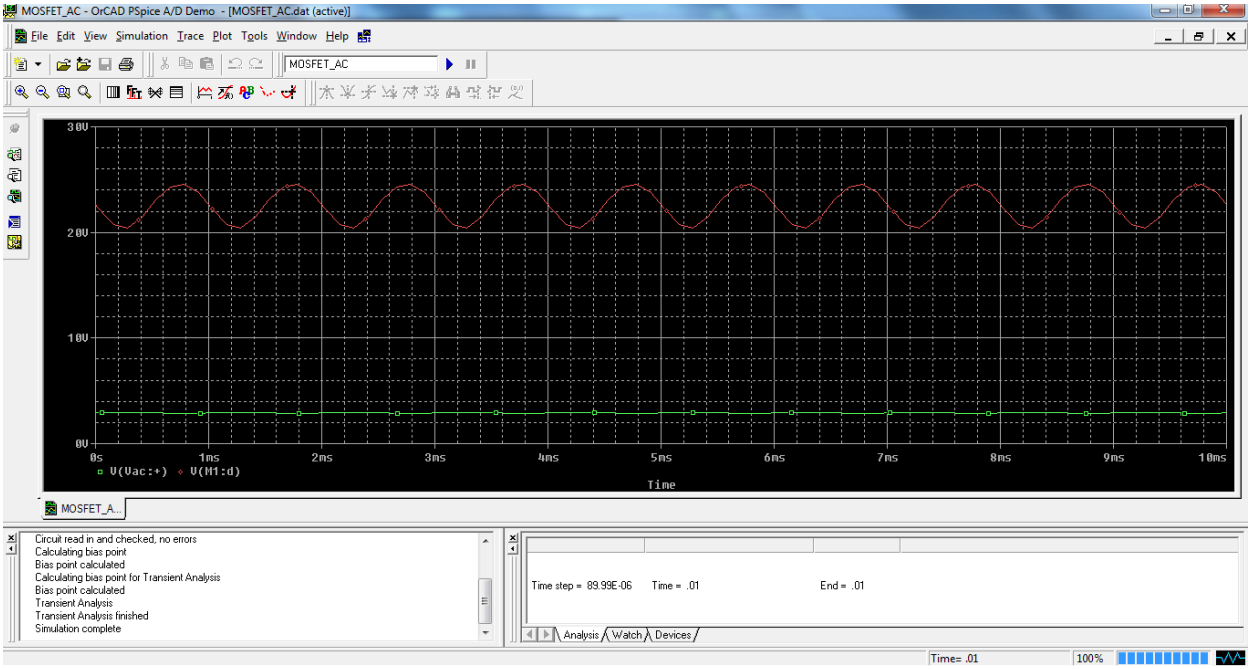


Fig.46.The input and output waveforms for the small signal AC amplifier with n-channel MOSFET

The RMS values for the input (gate) and output (drain) amplitudes may be monitored by selecting: *(MAX(V(M1:g))- MIN(V(M1:g)))/(2*SQRT(2))* for the gate terminal and: *(MAX(V(M1:d))- MIN(V(M1:d)))/(2*SQRT(2))* for the drain terminal (Fig.47).

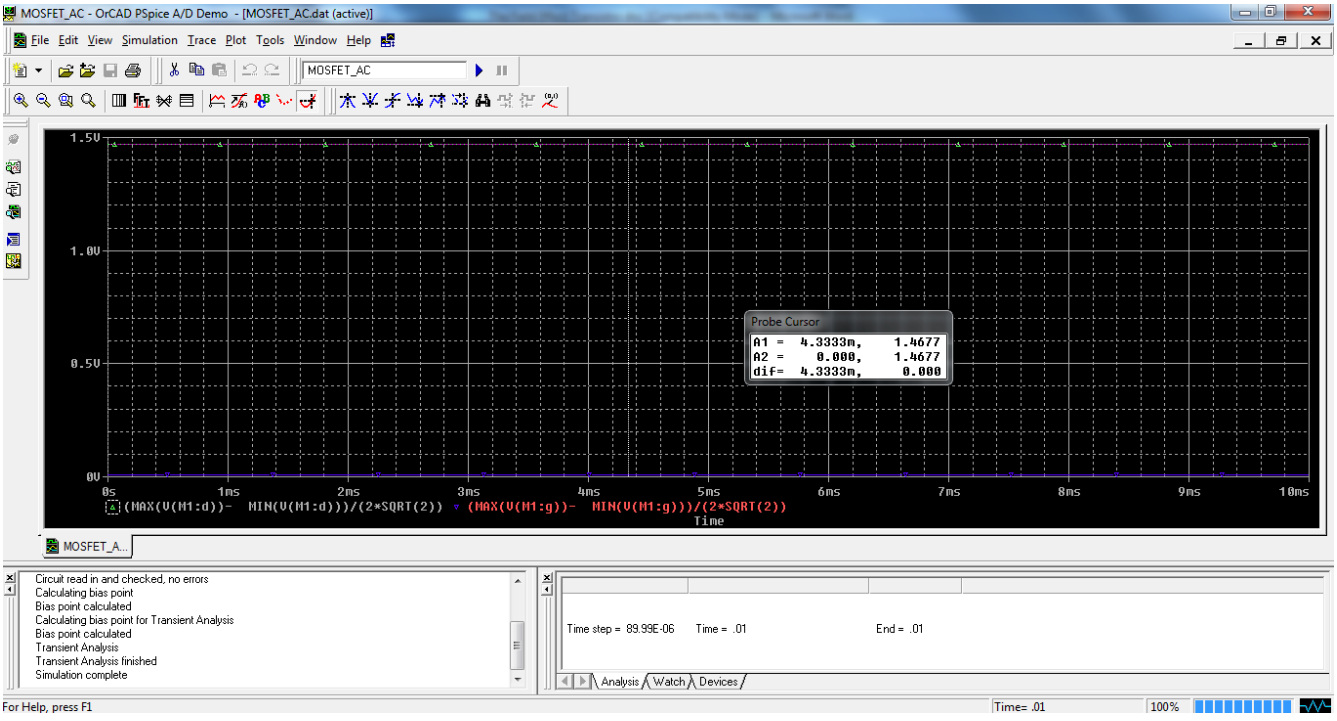


Fig.47.The RMS voltages for the small signal AC amplifier with n-channel MOSFET

By using Eq. 16-19, the AC gains for the amplifier may be calculated. The results will be displayed after the calculus in *Table 7*.

Table 7

RMS values	A_V	A_I	$A_Z(k\Omega)$	$A_Y(k\Omega^{-1})$
V_g(mV)=				
V_d(mV) =				
I_g(mA) =				
I_d(mA) =				

Exercises

1. Compare the AC gains for the JFET and the MOSFET amplifiers.
2. Measure and compare the input impedance for the JFET and for the MOSFET amplifiers.
3. What is the phase shift between the output and the input signals for the JFET and for the MOSFET amplifiers?
4. Compare the drain DC currents for the JFET and the MOSFET.

Annex 1

Table 8

Pos.	Component type	Value	Library
1.	R (resistor)	Numerical value is taken from the laboratory platform. - Mili-ohms if *m* is written after the numerical value - Ohms if nothing is written after the numerical value - Kilo-ohms if *k* is written immediately after the numerical value - Mega-ohms if *meg* is written immediately after the numerical value	Analog.slb
2.	J1	J2N3819 (n-JFET)	Eval.slb
3.	M1	IRF150 (n-MOSFET)	Eval.slb
4.	VSIN (used to function as a signal generator, sine-wave voltage source for time domain analysis)	- **DC**: the DC component of the sine wave - **AC**: the AC value of the sine wave. - **VOFF**: the DC offset value (set to zero if you need a pure sinusoid). - **VAMPL**: the undamped amplitude of the sinusoid; i.e., the peak value measured from zero if there were no DC offset value. - **FREQ**: the frequency in Hz of the sinusoid. - **TD**: the time delay in seconds (set to zero for the normal sinusoid). - **DF**: damping factor (set to zero for the normal sinusoid). - **PHASE**: phase advance in degrees (set to 90 if you need a cosine wave form). Note: the normal usage of this source type is to set **VOFF**, **TD** and **DF** to zero as this will give you a 'nice' sine wave.	Source.slb
5.	VDC (simple DC voltage source)	- Value in volts.	Source.slb
6.	GND_ANALOG	- Ground (node potential is 0 volts). - It is **mandatory** to be used in any PSpice schematic!	Port.slb

Bibliography

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