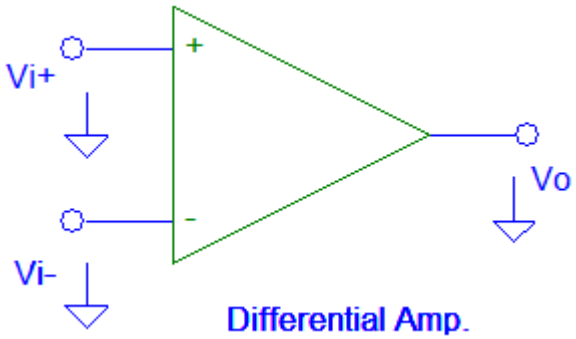
The Differential Amplifier

1. Introduction

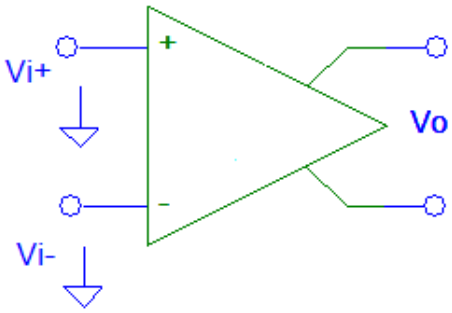
The differential amplifier is an analog circuit used to amplify the difference of two analog signals. Analog circuits are circuits dealing with input or output signals free to vary from zero until the supply voltage of the circuit. The differential amplifier is the basic input block of the operational amplifier, which is an analog integrated circuit. The integrated circuit **(IC,** and also called **microelectronic circuit**, **microchip**, or **chip**) is an assembly of electronic components, fabricated as a single unit, in which miniaturized active devices (e.g., transistors and diodes) and passive devices (e.g., capacitors and resistors) and their interconnections are built up on a thin substrate of semiconductor material (typically silicon). The resulting circuit is thus a small monolithic "chip," which may be as small as a few square centimeters or only a few square millimeters. The individual circuit components are generally microscopic in size.

2. Brief theory

The block diagram for a differential amplifier is presented in Fig.1.



a)



b)

Fig.1. The block diagram of the differential amplifier

The differential amplifier is a voltage amplifier. It has two inputs and one or two outputs. There are:

- The non-inverting input (+);
- The inverting input (-);
- An asymmetrical output when the amplifier has a single output terminal (Fig.1, a) or a symmetrical output (Fig.1, b) when the output signal is picked up between two output terminals of the amplifier, except ground. For the first case (single output), the amplifier is a standard differential amplifier. In the second situation (two outputs), the amplifier is named fully differential amplifier.

The function of the differential amplifier is to amplify the difference between the two input signals. The output voltage is proportional to the difference between the input voltages applied to the non-inverting and inverting inputs:

$$V_O = A \cdot (V_{i+} - V_{i-}) \quad (1)$$

,where A is the voltage gain of the amplifier.

The differential amplifiers are widely used to suppress the noise. Noise consists of typical differential noise and common-mode noise. There are two main causes of common-mode noise:

- Noise is generated in the wires and cables, due to electromagnetic induction, etc., and it causes a difference in potential (i.e., noise) between the signal source ground and the circuit ground.
- Current flowing into the ground of a circuit from another circuit causes a ground potential rise (noise).

In either case, the ground potential, a reference for a circuit, fluctuates because of noise. It is difficult to remove common-mode noise with typical filters. Differential amplifiers are used as a means of suppressing common-mode noise. In Fig.2 are represented from an architectural point of view the input and output sections of a differential amplifier. A common mode input voltage (V_{ic}) shapes the noise picked up from the outside on the two inputs. It is defined as the average voltage which is applied to the inputs. A differential input voltage (V_{id}) is applied between the non-inverting (+) and inverting (-) inputs to be amplified by the differential amplifier internal circuitry.

The main advantages of the differential amplifiers are:

- They amplify only difference-mode signals;
- They are easy to interconnect and cascade;
- They help us eliminate coupling capacitors;
- They are optimally suited to integration.

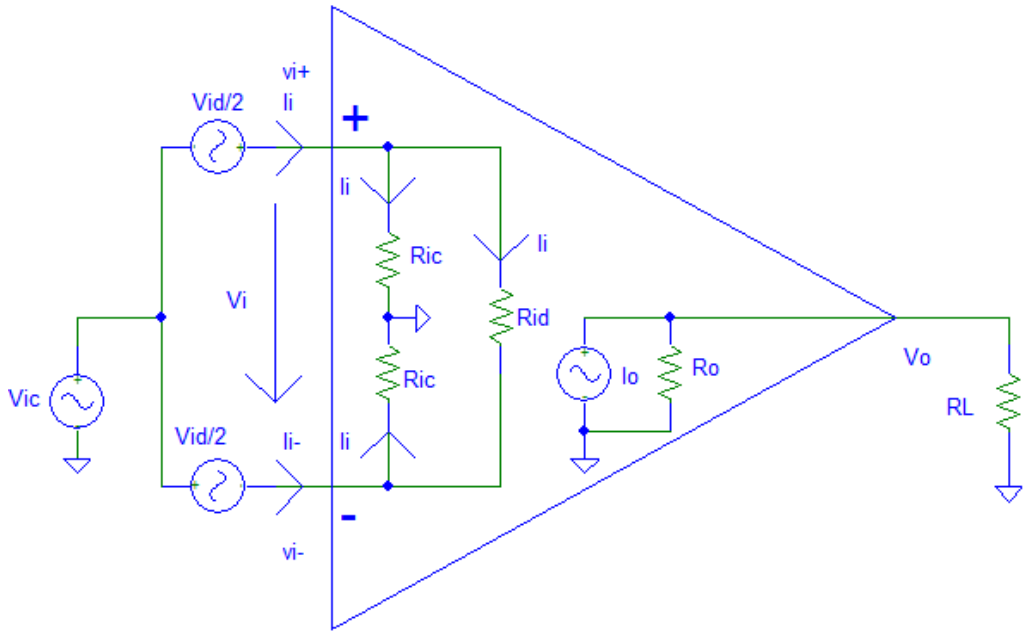


Fig.2.The internal architecture for the differential amplifier

The following equations can be written:

$$v_i^+ = v_{i,c} + \frac{v_{i,d}}{2} \quad (2)$$

$$v_i^- = v_{i,c} - \frac{v_{i,d}}{2} \quad (3)$$

The input currents into the non-inverting and the inverting inputs can be expressed according to the common mode and the differential mode input currents:

$$i_{i+} = i_{i,c} + i_{i,d} \quad (4)$$

$$i_{i-} = i_{i,c} - i_{i,d} \quad (5)$$

From the Eq. (2÷5), the following parameters are obtained:

- The differential input voltage:

$$v_{id} = v_i^+ - v_i^- \quad (6)$$

- The common mode input voltage:

$$v_{ic} = \frac{v_i^+ + v_i^-}{2} \quad (7)$$

- The differential input current:

$$i_{id} = \frac{i_i^+ - i_i^-}{2} \quad (8)$$

- The common mode input current:

$$i_{ic} = \frac{i_i^+ + i_i^-}{2} \quad (9)$$

a. Pure differential input mode

For the pure differential input situation, the common mode parameters are removed:

$$v_{ic} = 0\,,\ i_{ic} = 0 \quad (10)$$

In this mode, the following equations are valid:

$$v_{id} = v_i^+ = -v_i^- \quad (11)$$

$$i_{id} = i_{i,+} = -i_{i,-} \quad (12)$$

The input impedance in the differential mode is:

$$R_{id} = \frac{v_{id}}{i_{id}} \quad (13)$$

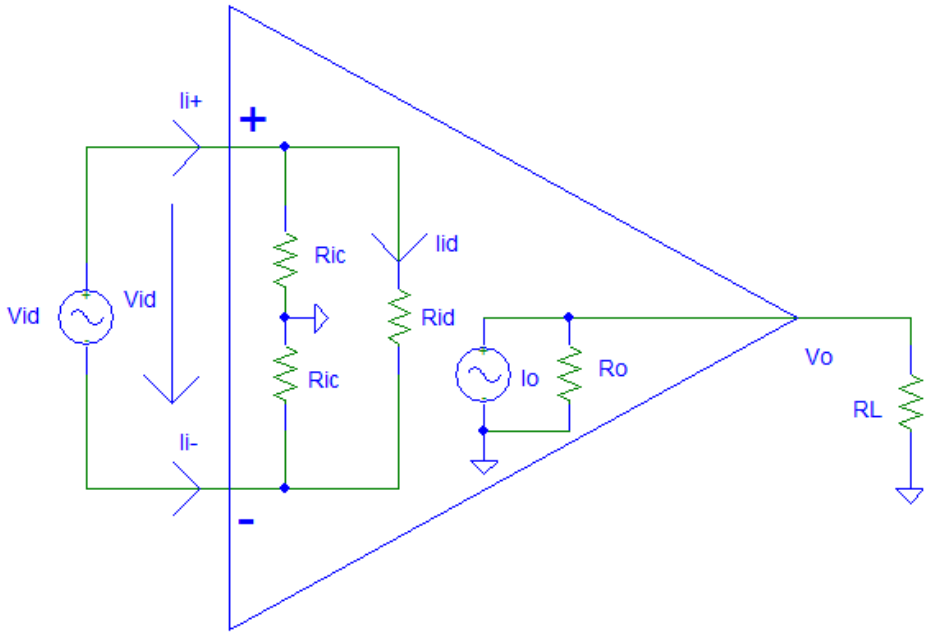


Fig.3.The differential amplifier internal architecture for the pure differential input mode

b. Pure common mode input

In the pure common mode input situation, the differential mode parameters are neglected:

$v_{id} = 0,\ i_{id} = 0$ (14)

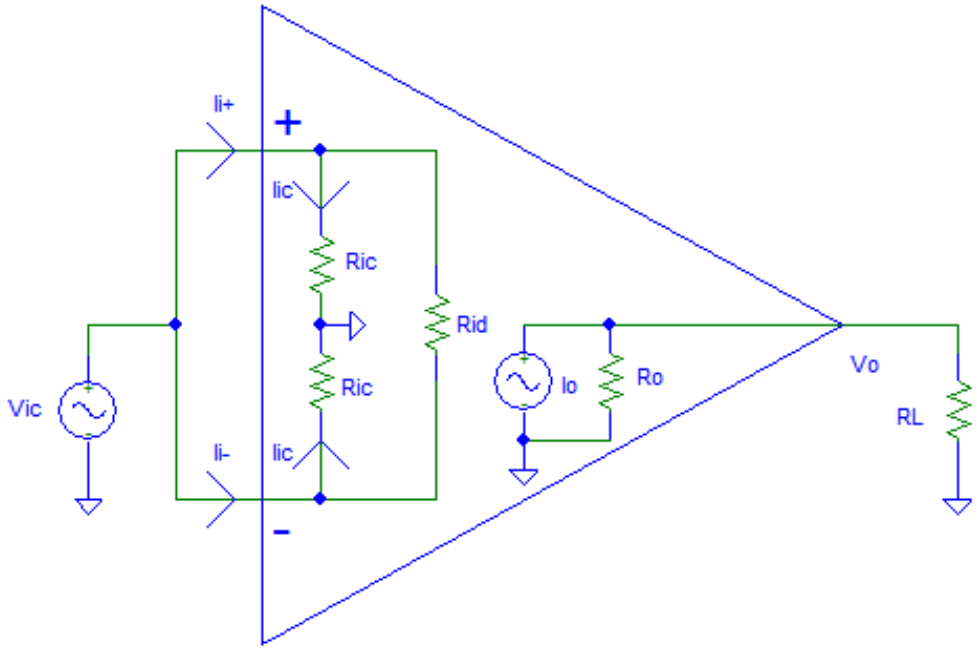


Fig.4.The differential amplifier internal architecture for the pure common mode input

In this mode, the eq. 15÷16 may be written:

$$v_{ic} = v_i^+ = v_i^- \quad (15)$$

$$i_{ic} = i_{i,+} = i_{i,-} \quad (16)$$

The input impedance in the common mode is:

$$R_{ic} = \frac{v_{ic}}{i_{ic}} \quad (17)$$

For a fully differential amplifier (the amplifier has two output terminals), the equations for the output voltages are:

$$v_{od} = v_o^+ - v_o^- \quad (18)$$

$$v_{oc} = \frac{v_o^+ + v_o^-}{2} \quad (19)$$

The voltage gain of a differential circuit which amplifies the difference between the two input signals is known as the differential gain (A_d):

$$A_d = \frac{v_{od}}{v_{id}} \quad (20)$$

The voltage gain of a differential circuit which amplifies the common mode input voltage applied to the two input signals is known as the common mode gain (A_c):

$$A_c = \frac{v_{oc}}{v_{ic}} \quad (21)$$

If the circuits built inside the differential amplifier connected to the non-inverting and inverting inputs are perfectly identical, the common mode gain (A_c) is zero, because both sections have the same behavior and amplify in the same way the signal applied to the inputs (v_{oc}=0). But, in practice, it is impossible to build two perfectly identical amplifiers, which means that there will be a non-zero common output voltage, and a small

common mode gain (which is even smaller as the two amplification stages have the closest parameters possible):

$$0 < |A_C| < 1 \quad (22)$$

The differential amplifier will amplify the difference between the voltages applied between the two inputs, and it will reject the common part of the input voltages. The ratio between the differential gain and the common mode gain is named the common mode rejection ratio (CMRR) and it is a very important parameter which describes the performance of the amplifier:

$$CMRR = \frac{|A_d|}{|A_c|} \quad (23)$$

Typically, the common mode rejection ratio (CMRR) of the differential amplifier is measured in decibels (dB) and it can have values between 40dB and 120dB.

The BJT differential amplifier

A differential amplifier with two NPN bipolar junction transistors is depicted in Fig.5. The transistors should have characteristics as identical as possible. The bias resistor connected in the emitters (R_E) could be replaced by a current source circuit built with BJT or FET, which offers a much greater output resistance and improved performance.

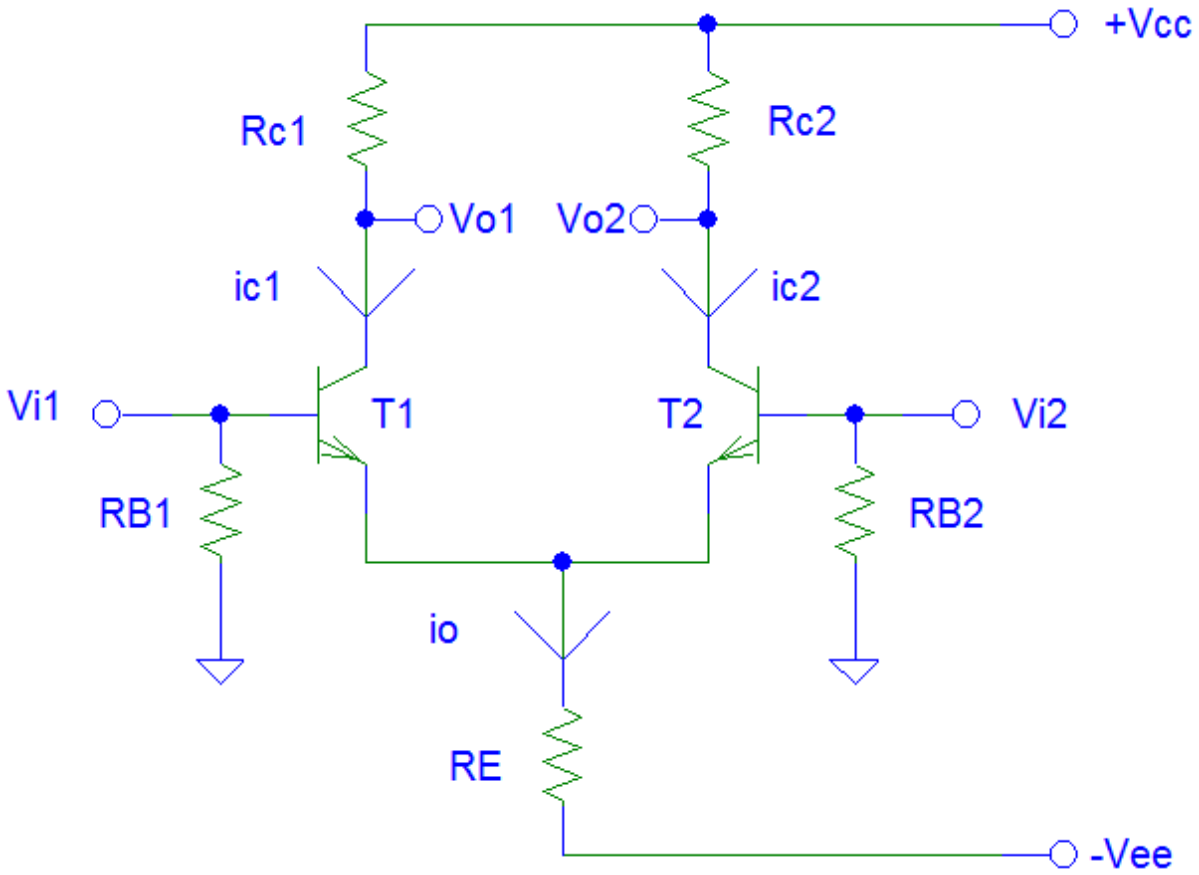


Fig.5.The differential amplifier with bipolar junction transistors

The output can be taken:

- Symmetrical ($R_{c1} = R_{c2} = R_c$):
  $v_O = v_{O1} - v_{O2} = A \cdot (v_{i1} - v_{i2})$ (24)
- Asymmetrical($R_{c1} = R_{c2} = R_c$):

$$v_O = v_{O1} \text{ or } v_O = v_{O2}; (25)$$
$$v_O = \pm A \cdot (v_{i1} - v_{i2}) \ (26)$$

Large signal analysis

For the circuit from Fig.5, write the equations:

$$I_O = i_{E1} + i_{E2} (27)$$
$$I_O \cong i_{C1} + i_{C2} (28)$$

By replacing the collector current, we have:

$$I_O = I_S \left(e^{\frac{v_{BE1}}{V_{th}}} + e^{\frac{v_{BE2}}{V_{th}}} \right) (29)$$
$$I_O = I_S e^{\frac{v_{BE1}}{V_{th}}} \left(1 + e^{\frac{v_{BE2} - v_{BE1}}{V_{th}}} \right) (30)$$

But:

$$i_{C1} = I_S e^{\frac{v_{BE1}}{V_{th}}} \quad (31)$$
$$v_{BE2} - v_{BE1} = v_{I2} - v_{I1}$$

It is possible to write the expressions of collector currents:

$$i_{C1} = \frac{I_O}{1 + e^{\frac{v_{I2} - v_{I1}}{V_{th}}}} = \frac{I_O}{2} \left(1 + th \frac{v_{I1} - v_{I2}}{2V_{th}} \right) (32)$$
$$i_{C2} = \frac{I_O}{1 + e^{\frac{v_{I1} - v_{I2}}{V_{th}}}} = \frac{I_O}{2} \left(1 - th \frac{v_{I1} - v_{I2}}{2V_{th}} \right) (33)$$

The collector currents i_{C1} and i_{C2} could be developed in Taylor series:

$$\frac{i_{C1}(x)}{I_O} = \frac{1}{1 + e^{-x}} = \frac{1}{2} + \frac{x}{4} - \frac{x^3}{48} + \ldots \ (34)$$
$$\frac{i_{C2}(x)}{I_O} = \frac{1}{1 + e^{x}} = \frac{1}{2} - \frac{x}{4} + \frac{x^3}{48} - \ldots (35)$$

,where:

$$x = \frac{v_{i1} - v_{i2}}{V_{th}} \ (36)$$

So, the tangent at characteristic $i_{C1}(x)/I_O$ has the following equation:

$$y = \frac{1}{2} + \frac{x}{4} \ (37)$$

If $y = 0 \Rightarrow x = -2 \Rightarrow v_{I1} - v_{I2} = -2V_{th} = -50mV$.

Remarks:

- for $v_{I1} = v_{I2}$ (or x = 0), $i_{C1} = i_{C2} = I_O/2$
- for a quasi-linear operation, the maximal amplitude of the input voltage must be less than $2V_{th}$ (or x =2), so about 50mV

The static characteristic for the BJT differential amplifier is represented in Fig.6.

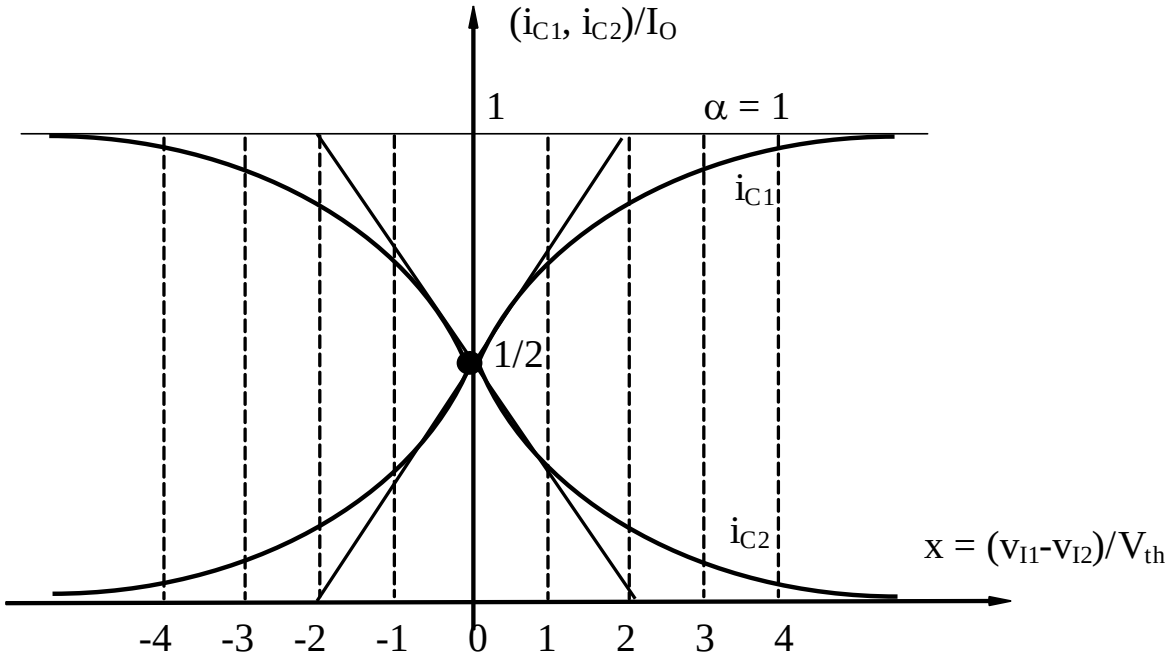


Fig.6. The static characteristics $(i_{C1}, i_{C2})/I_O = f\,[(v_{i1}-v_{i2})/V_{th}]$ for the differential amplifier

The output symmetrical voltage is:

$$v_O = v_{O1} - v_{O2} = \left(i_{C2} - i_{C1}\right) R_C = \left(-\frac{x}{2} + \frac{x^3}{24} - ... \right) I_O R_C \quad (38)$$

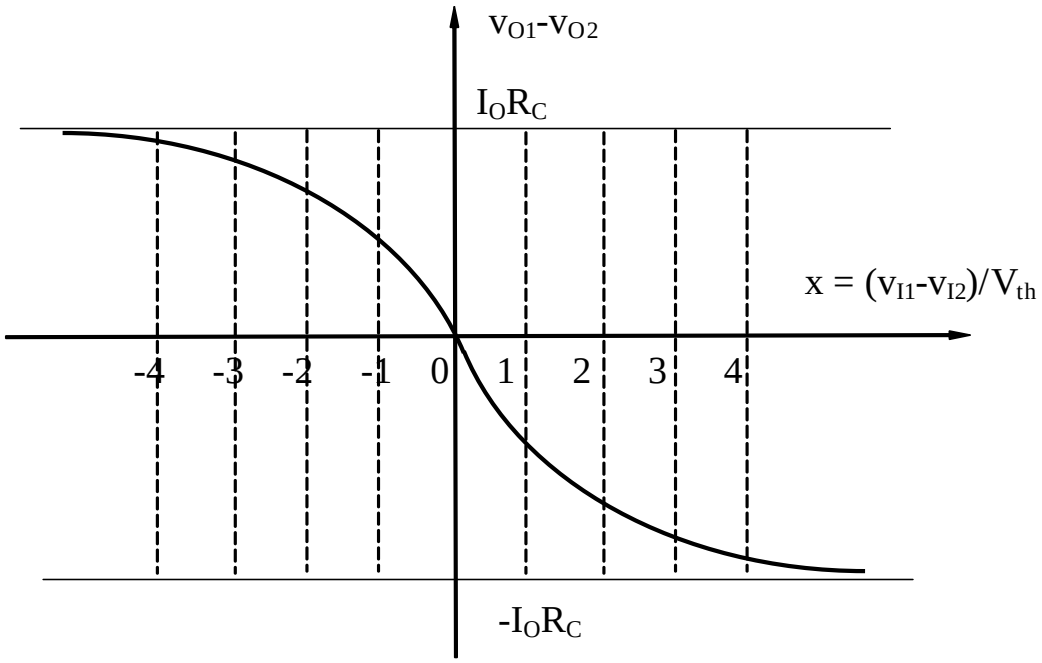


Fig.7.The static characteristic $v_{O1}-v_{O2} = f\,[(v_{I1}-v_{I2})/V_{th}]$ for the differential amplifier

It is possible to increase the maximum range of the input voltage (for a linear operation of the circuit) by inserting two resistances in emitters (emitter degeneration).

Small signal analysis

The pairs of the signals which are present at the inputs and at the outputs of the differential amplifier can be decomposed into a portion that is the identical in both, and a portion that is equal, but opposite in both. For example, if we have two voltages, v_1 and v_2 , we can define a common-mode signal, v_c, and a difference-mode signal, v_d, as:

$$v_c = \frac{v_1 + v_2}{2} \quad (39)$$

$$v_d = v_1 - v_2 \quad (40)$$

In terms of these two voltages, we can write v_1 and v_2 as:

$$v_1 = v_c + \frac{v_d}{2} \quad (41)$$

$$v_2 = v_c - \frac{v_d}{2} \quad (42)$$

In incremental analysis of linear amplifiers we will decompose our inputs into difference-and common-mode inputs:

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} \quad (43)$$

$$v_{id} = v_{i1} - v_{i2} \quad (44)$$

We will apply v_{id} to the circuit and get $v_{od} = A_d \cdot v_{id}$, and then apply v_{ic} to get $v_{oc} = A_c \cdot v_{ic}$ .Then we will reconstruct our outputs:

$$v_{o1} = v_{oc} + \frac{v_{od}}{2} = A_c \cdot v_{ic} + A_d \cdot \frac{v_{id}}{2} \ , \ v_{o1} = v_{oc} - \frac{v_{od}}{2} = A_c \cdot v_{ic} - A_d \cdot \frac{v_{id}}{2} \quad (45)$$

The differential amplifier can be seen as a circuit with linear response when a small signal (less than $2V_{th}$) is applied to its inputs (Fig.8).

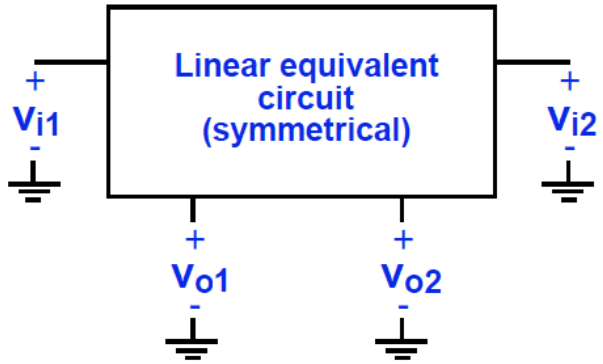


Fig.8. The differential amplifier regarded as a linear (symmetrical) circuit

Because of its internal symmetry, the circuit may be divided in two identical sections(Fig.9).

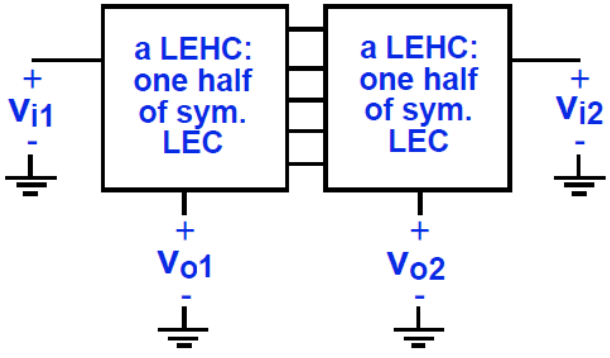


Fig.9. The differential amplifier divided in two identical blocks

For the analysis of the amplifier in the differential mode, the common links between the identical sections of the differential amplifier are grounded (Fig.10).

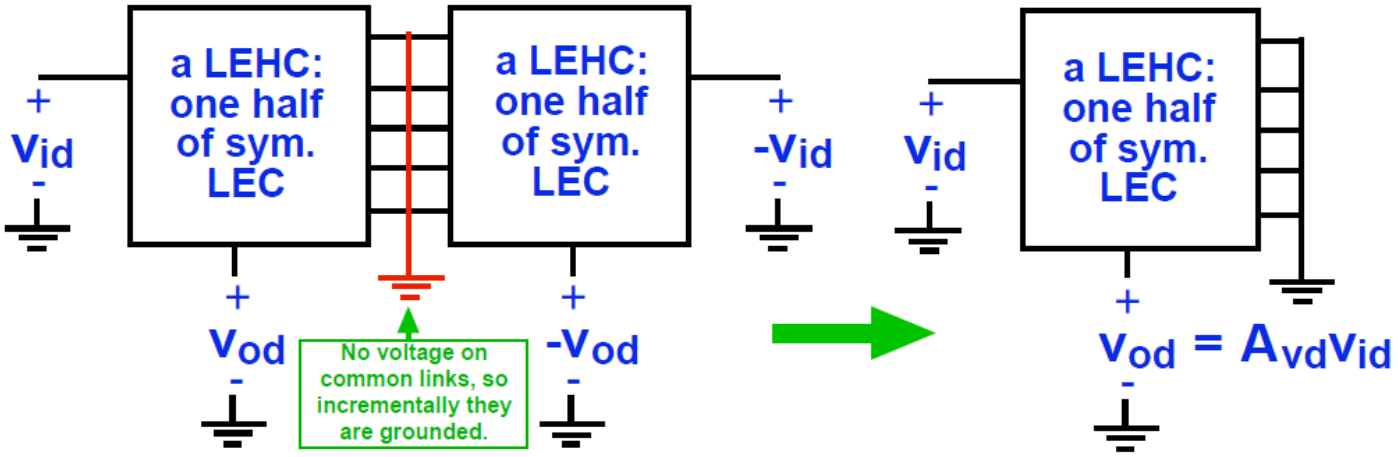


Fig.10. The amplifier in differential mode

By applying the rule, the BJT differential amplifier will be the one in Fig.11.

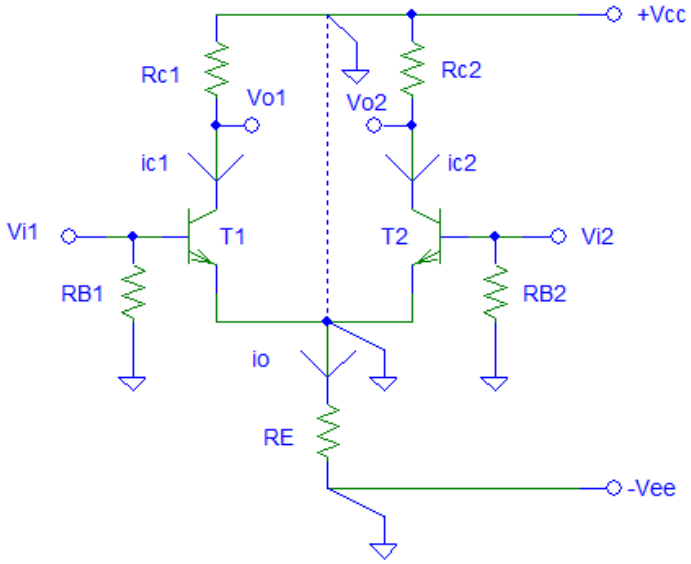


Fig.11. The BJT amplifier in differential mode

To calculate the differential gain, take half of the circuit:

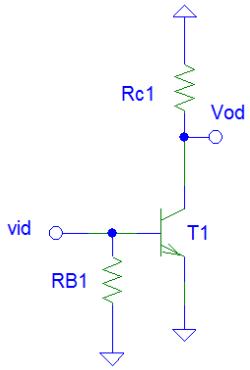


Fig.12. The circuit for the calculus of the differential gain

The differential gain is:

$$A_d = \frac{v_{od}}{v_{id}} = \frac{-g_m \cdot v_{id} \cdot R_{c1}}{v_{id}} = -g_m \cdot R_{c1} \quad (46)$$

For a symmetrical output, we have:

$$A = \frac{2v_{od}}{2v_{id}} = A_d \quad (47)$$

For an asymmetrical output, the gain is:

$$A = \frac{v_{od}}{2v_{id}} = \frac{A_d}{2} \quad (48)$$

The differential input resistance is:

$$R_{id} = 2 \cdot (r_\pi \,||\, R_{B1}) \quad (49)$$

For the analysis of the amplifier in the common mode, the common links between the identical sections of the differential amplifier are removed (Fig.13).

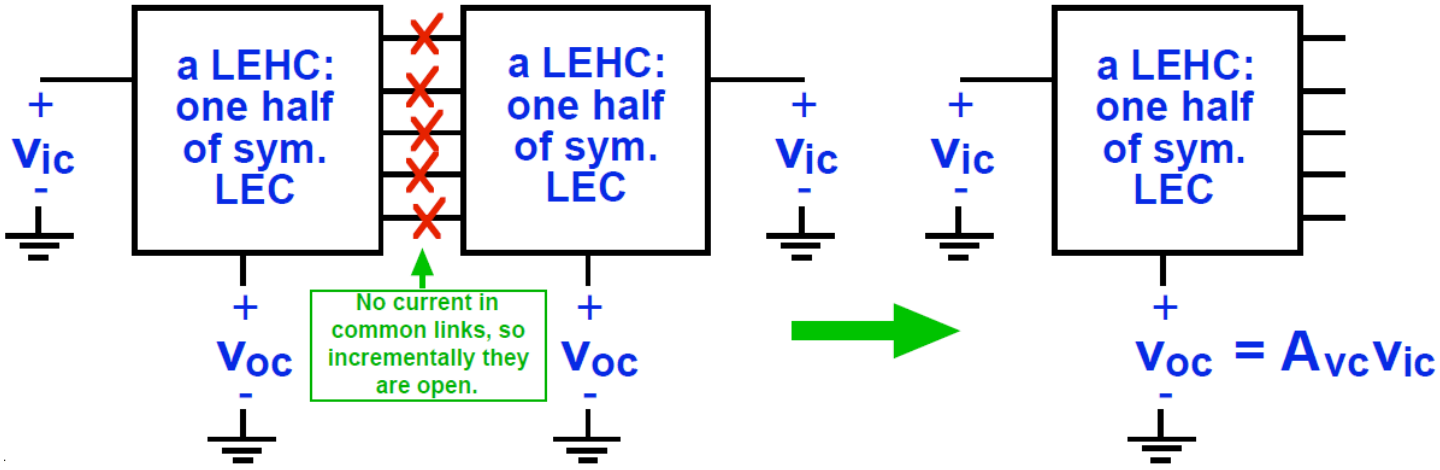


Fig.13. The amplifier in common mode configuration

By applying the rule presented above, the BJT differential amplifier will be the one in Fig.14.

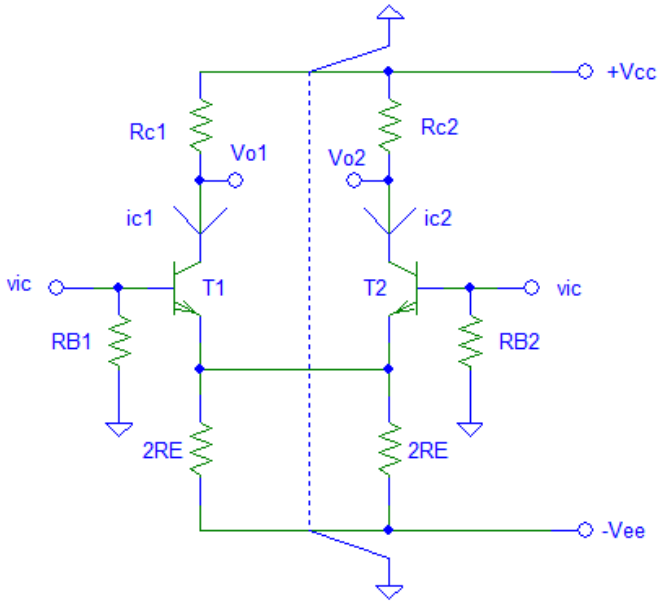


Fig.14. The amplifier in common mode configuration

To calculate the common mode gain, take half of the circuit:

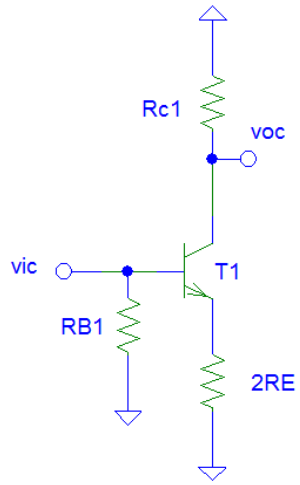


Fig.15. The circuit for the calculus of the common mode gain

The common mode gain is:

$$A_c = \frac{v_{oc}}{v_{ic}} = \frac{-g_m \cdot v_{be} \cdot R_{c1}}{v_{be} \cdot \left[1 + 2 \cdot R_E \cdot \left(g_m + \frac{1}{r_{\pi 1}}\right)\right]} = \frac{-g_m \cdot R_{c1}}{1 + 2 \cdot R_E \cdot \left(g_m + \frac{1}{r_{\pi 1}}\right)} \cong -\frac{R_{c1}}{2R_E} \quad (50)$$

The input resistance in the common mode configuration is:

$$R_{ic} = \frac{v_{ic}}{i_{ic}} = R_{B1} \| \left[r_\pi + 2 \cdot R_E \cdot (\beta_0 + 1)\right] \quad (51)$$

The CMRR is:

$$CMRR = \frac{A_d}{A_c} = 1 + 2 \cdot R_E \cdot \left(g_m + \frac{1}{r_{\pi 1}}\right) \cong g_m \cdot 2R_E \quad (52)$$

To increase the CMRR, the resistor R_E may be replaced by a current source.

3. Laboratory activity

a. DC bias of the differential amplifier.

Consider the circuit from Fig.16. Draw the circuit. The potentiometer has the following parameters: VALUE=1k, SET=0.49. Measure the collector currents and the DC voltages in the collector of T_1 and T_2.

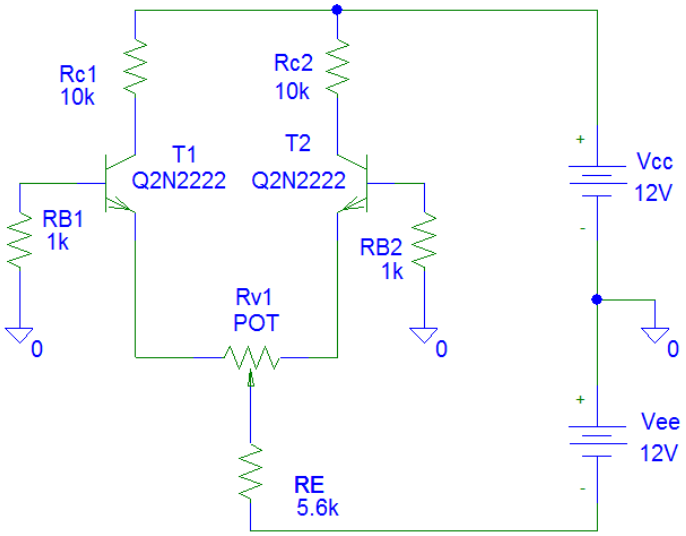


Fig.16. The differential amplifier – the DC bias

Table 1

I_{C1}(mA)=	V_{C1}(V)=
I_{C2}(mA)=	V_{C2}(V)=

b. The differential gain in DC

Draw the circuit from Fig.17. The voltage source (V1) has the parameters mentioned in Fig.18. Measure the DC differential output voltage (the difference between the potentials in the collectors of T_1 and T_2). The results should be written in *Table 2*.

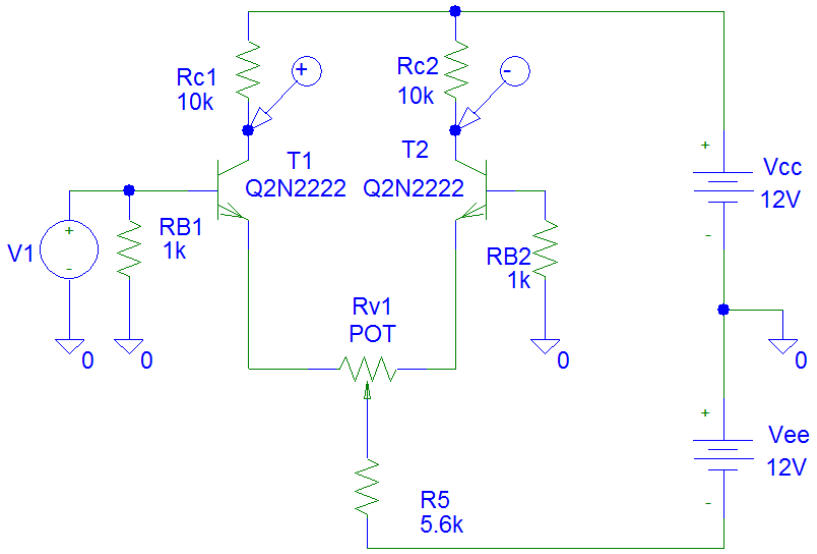


Fig.17. The differential gain of the amplifier in DC

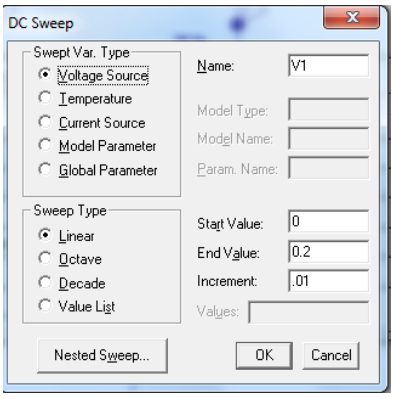


Fig.18. The DC sweep settings for V1

Table 2

V_1 (mV)	$\lvert V_{C1}-V_{C2}\rvert$(mV)	A_d
0		-
50		
100		
150		
200		

c. The common mode gain in DC

Consider the circuit from Fig.19. V_1 has the same parameter as for differential mode. Measure the difference between the potentials in the collectors of T_1 and T_2. The results should be collected in *Table 3*.

Table 3

V_1 (mV)	$\|V_{C1}-V_{C2}\|$(mV)	A_c
0		-
50		
100		
150		
200		

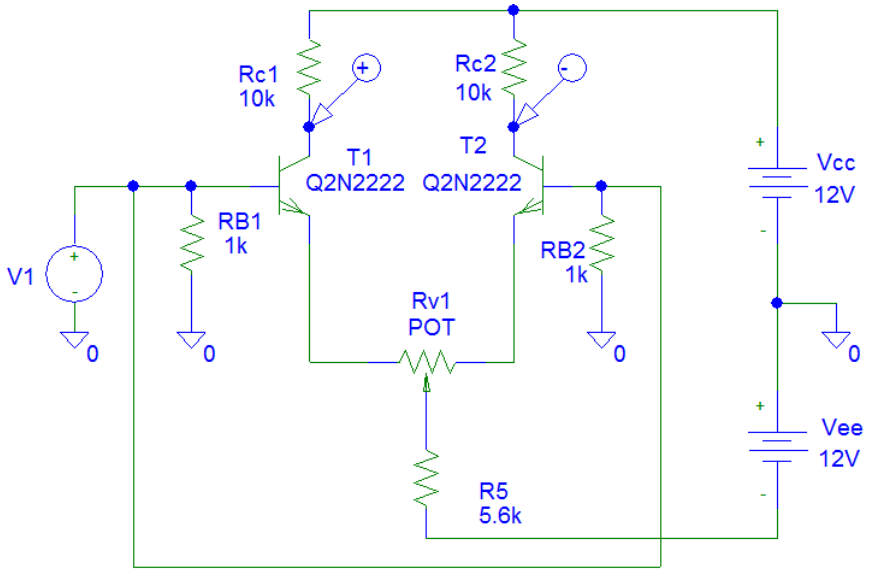


Fig.19. The common mode gain of the amplifier in DC

Calculate the CMRR. The results are written in Table 4.

Table 4

V_1 (mV)	CMRR
0	-
50	
100	
150	
200	

d. The AC differential gain

Draw the circuit from Fig.20. V_{in} is a sine wave voltage source (VSIN) with the following parameters: *VOFF=0; VAMPL=100m; FREQ=1k*. The potentiometer has the parameters VALUE=1k, SET=0.5. The simulation should be performed in the time domain (transient) with a *Final Time=5ms*. Measure the potentials in the collectors of T_1 and T_2. The results are written in *Table 5*.

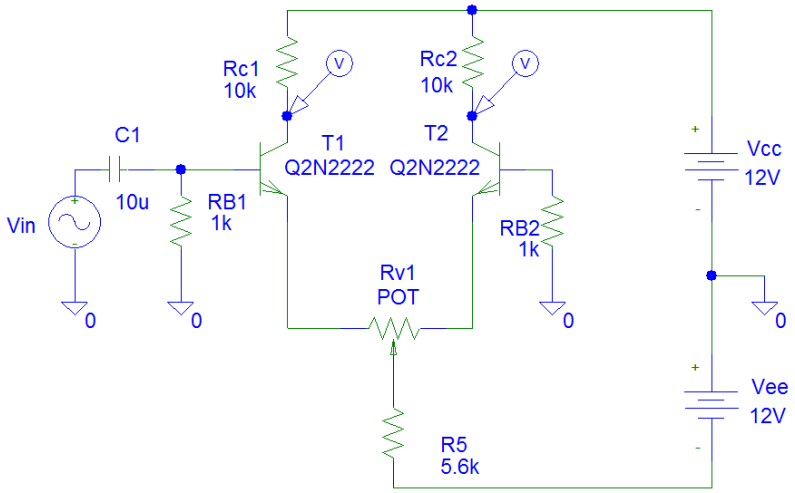


Fig.20. The circuit for the calculus of the AC differential gain

Table 5

V_{in} (mV)	100	A	ΔΦ
V_{C1}(mV)			
V_{C2}(mV)			

e. The differential input resistance (R_{id})

Consider the circuit from Fig.21, which is obtained based on the circuit in Fig.20. The differential input resistance is given by:

$$R_{id} = \frac{\underline{V_i}}{\underline{I_i}} = \frac{\underline{V_{b1}}}{\underline{V_{in}} - \underline{V_{b1}}} \cdot R_g \quad (53)$$

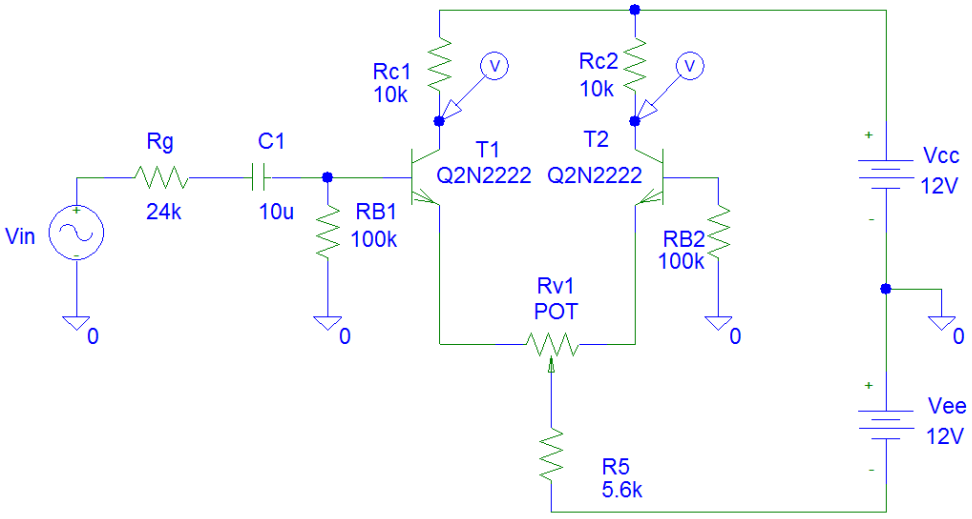


Fig.20. The circuit for the calculus of the differential input resistance

The results are written in Table 6.

Table 6

$\underline{V_{in}}$ (mV)	$\underline{V_{b1}}$ (mV)	R_{id}(kΩ)
100		

f. The common mode input resistance (R_{ic})

Let's consider the circuit from Fig.22. The common mode input resistance is given by:

$$R_{ic} = \frac{\underline{V_i}}{\underline{I_i}} = \frac{\underline{V_{b1}}}{\underline{V_{in}} - \underline{V_{b1}}} \cdot R_g \quad (54)$$

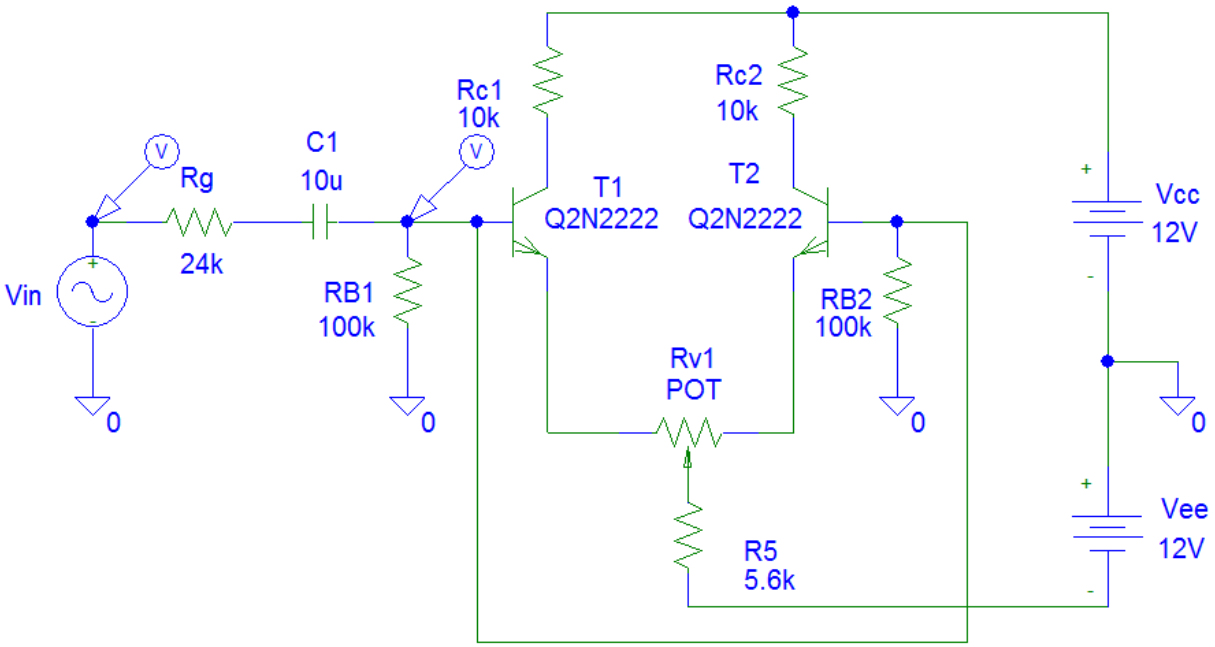


Fig.22. The circuit for the calculus of the common mode input resistance

The results are written in Table 7.

Table 7

$\underline{V_{in}}$ (mV)	$\underline{V_{b1}}$ (mV)	R_{ic}(kΩ)
100		

Annex 1

Table 1

Pos.	Component type	Value	Library
1.	R (resistor)	Numerical value is taken from the laboratory platform. - Mili-ohms if *m* is written after the numerical value - Ohms if nothing is written after the numerical value - Kilo-ohms if *k* is written immediately after the numerical value - Mega-ohms if *meg* is written immediately after the numerical value	Analog.slb
2.	C (capacitor)	Numerical value is taken from the laboratory platform. - Pico-farads if *p* is written after the numerical value - nano-farads if *n* is written after the numerical value - micro-farads if *u* is written after the numerical value - mili-farads if *m* is written after the numerical value - farads if nothing is written after the numerical value	Analog.slb
3.	VSRC	Simple voltage source: AC, DC, Transient may be specified	Source.slb
4.	VSIN (used to function as a signal generator, sine-wave voltage source for time domain analysis)	- **DC**: the DC component of the sine wave - **AC**: the AC value of the sine wave. - **VOFF**: the DC offset value (set to zero if you need a pure sinusoid). - **VAMPL**: the undamped amplitude of the sinusoid; i.e., the peak value measured from zero if there were no DC offset value. - **FREQ**: the frequency in Hz of the sinusoid. - **TD**: the time delay in seconds (set to zero for the normal sinusoid). - **DF**: damping factor (set to zero for the normal sinusoid). - **PHASE**: phase advance in degrees (set to 90 if you need a cosine wave form). Note: the normal usage of this source type is to set **VOFF**, **TD** and **DF** to zero as this will give you a 'nice' sine wave.	Source.slb
5.	VDC (simple DC voltage source)	- Value in volts.	Source.slb
6.	GND_ANALOG	- Ground (node potential is 0 volts). - It is **mandatory** to be used in any PSpice schematic!	Port.slb
7.	Q2N2222	NPN transistor	Eval.slb
8.	Q2N3904	NPN transistor (pair for 2N2222 to unbalance the differential stage, if necessary)	Eval.slb
9.	POT	Potentiometer, default values: VALUE =1K; SET =0.5 (SET may be 0.49 to unbalance the differential stage, if necessary)	Breakout.slb

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