SIMPLE RISC PROCESSOR MICROARCHITECTURE

v.1.0

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1. Processor pipeline:

The Simple RISC Processor main blocks are sketched in figure 1.

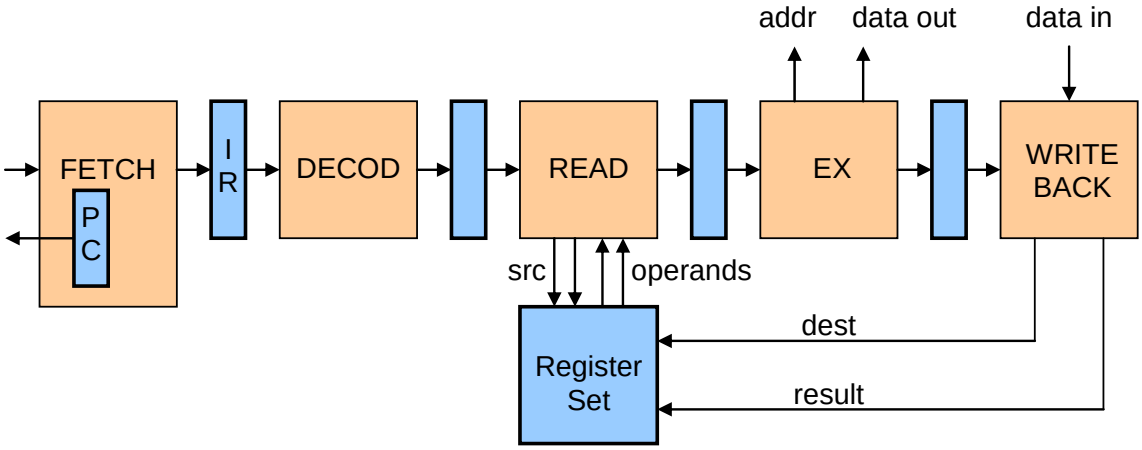

Figure 1
Simple RISC Processor Pipeline.
ISA registers and pipeline registers are shaded in blue.

The processor has a 5 stages pipeline. The fetch stage keeps and updates the program counter (PC) and reads instructions from the program memory. Its output may be assimilated with the instruction register (IR). The read stage fetches the instruction operands from the register set. The execution stage does the actual computation for the arithmetic and logic instructions and delivers the memory address (addr) for load/store instructions. It delivers also the data to be sent to the memory (data out) for the store instruction. The last stage, write back, sends back the result to the register set and samples the data from the memory output for a load instruction (data in).

It is assumed that the data memory is synchronous with a latency of two clock cycles. It samples the address input at the end of the first cycle, and delivers the corresponding data during the next cycle (it must be sampled at the end of this second cycle).