Capitolul 5

Etaje de iesire

5.1. Notiuni generale

5.1. Caracteristici generale

- debiteaza putere intr-o sarcina, avand un randament ridicat si putere disipata redusa pe tranzistoarele finale
- impedanta redusa de iesire
- excursie maxima a tensiunii de iesire
- distorsiuni minime

Clasa A:

- distorsiuni foarte reduse
- randament redus

Clasa B:

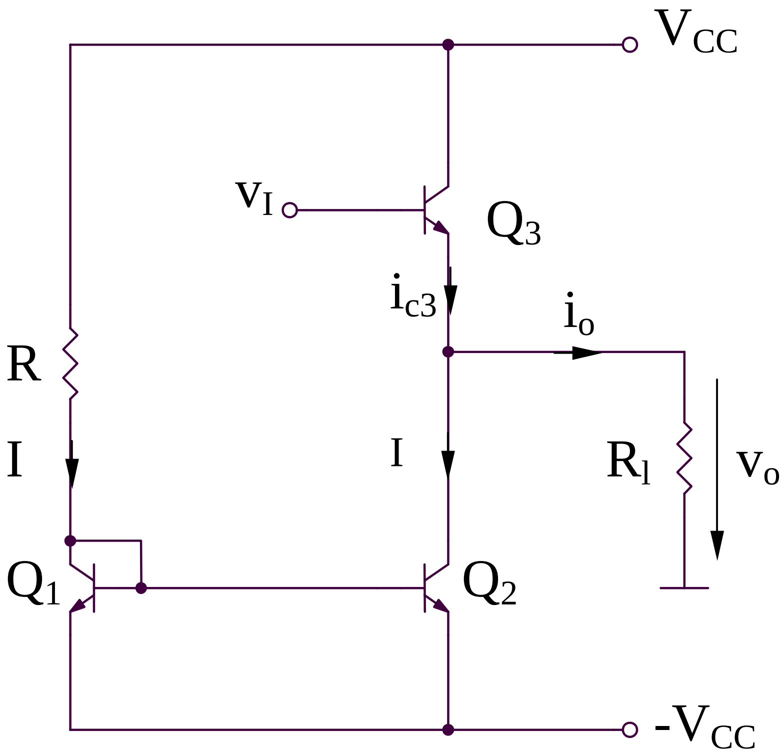
- distorsiuni importante
- randament foarte bun

Clasa AB:

- distorsiuni reduse
- randament bun

5.2. Etajul de iesire in clasa A, configuratie colector comun

5.2. Etajul de iesire in clasa A, configuratie colector comun



In repaus:

$$v_O = 0; i_O = 0$$

$$I_{C3} = I; V_{CE3} = V_{CC}$$

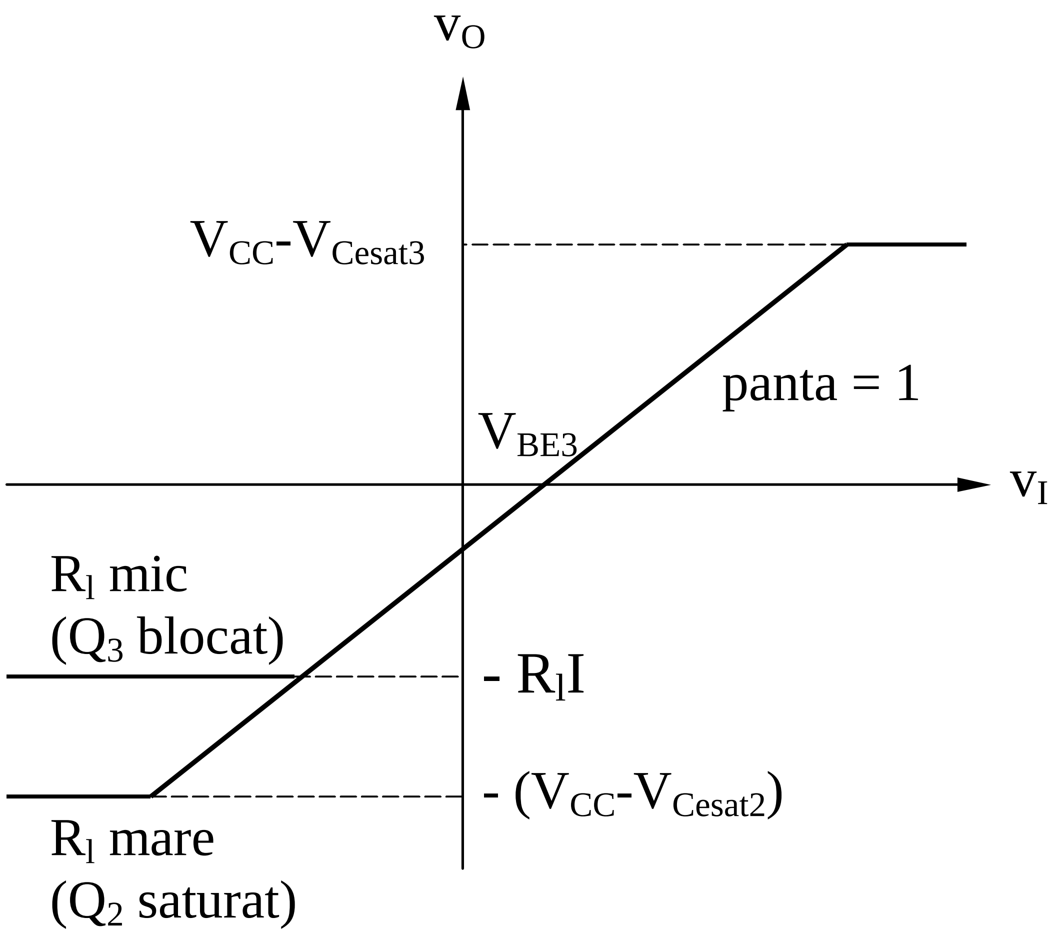
$$V_I = V_{BE3} = V_{th} \ln\left(\frac{I}{I_S}\right)$$

Caracteristica de transfer $v_O = f(v_I)$

$$\left.\begin{aligned} v_I &= v_{BE3} + v_O \\ v_{BE3} &= V_{th} \ln\left(\frac{i_{c3}}{I_S}\right) \\ i_{c3} &= I + \frac{v_O}{R_l} \end{aligned}\right\} \Rightarrow v_I = v_O + V_{th} \ln\left(\frac{I + \frac{v_O}{R_l}}{I_S}\right)$$

Cu $\frac{v_O}{R_l} << I, V_{th} \ln\left(\frac{I}{I_S}\right) = V_{BE3}$, expresia caracteristicii de transfer

devine, in consecinta $v_I = v_O + v_{BE3}$, deci liniara.



$$i_{C3} = I + \frac{v_O}{R_l}$$

$$i_{C3} = I + \frac{V_{CC} - v_{CE3}}{R_l}$$

$$i_{C3} = 0 \Rightarrow v_{CE3} = V_{CC} + IR_l$$

Valoarea maxima pozitiva a tensiunii de iesire este:

$$V_{OM}^{+} = V_{CC} - V_{CEsat3}$$

Valoarea maxima negativa a tensiunii de iesire depinde de valoarea R_l:

- pentru valori mari ale R_l, limita negativa a tensiunii de iesire este data de saturatia tranzistorului Q_2

$$|V_{OM}^{-}| = V_{CC} - V_{CEsat2}$$

- pentru valori mici ale R_l, limita negativa a tensiunii de iesire este data de blocarea tranzistorului Q_2

$$|V_{OM}^{-}| = IR_l < V_{CC} - V_{CEsat2}$$

Relatii energetice fundamentale

Notand:

$$\hat{V}_O = KV_{CC}$$

K fiind factorul de utilizare a tensiunii de alimentare, 0 ≤ K < 1. Deci:

$$\hat{I}_O = \frac{\hat{V}_O}{R_l} = \frac{KV_{CC}}{R_l} = KI$$

Puterea disipata pe tranzistorul Q_3 este:

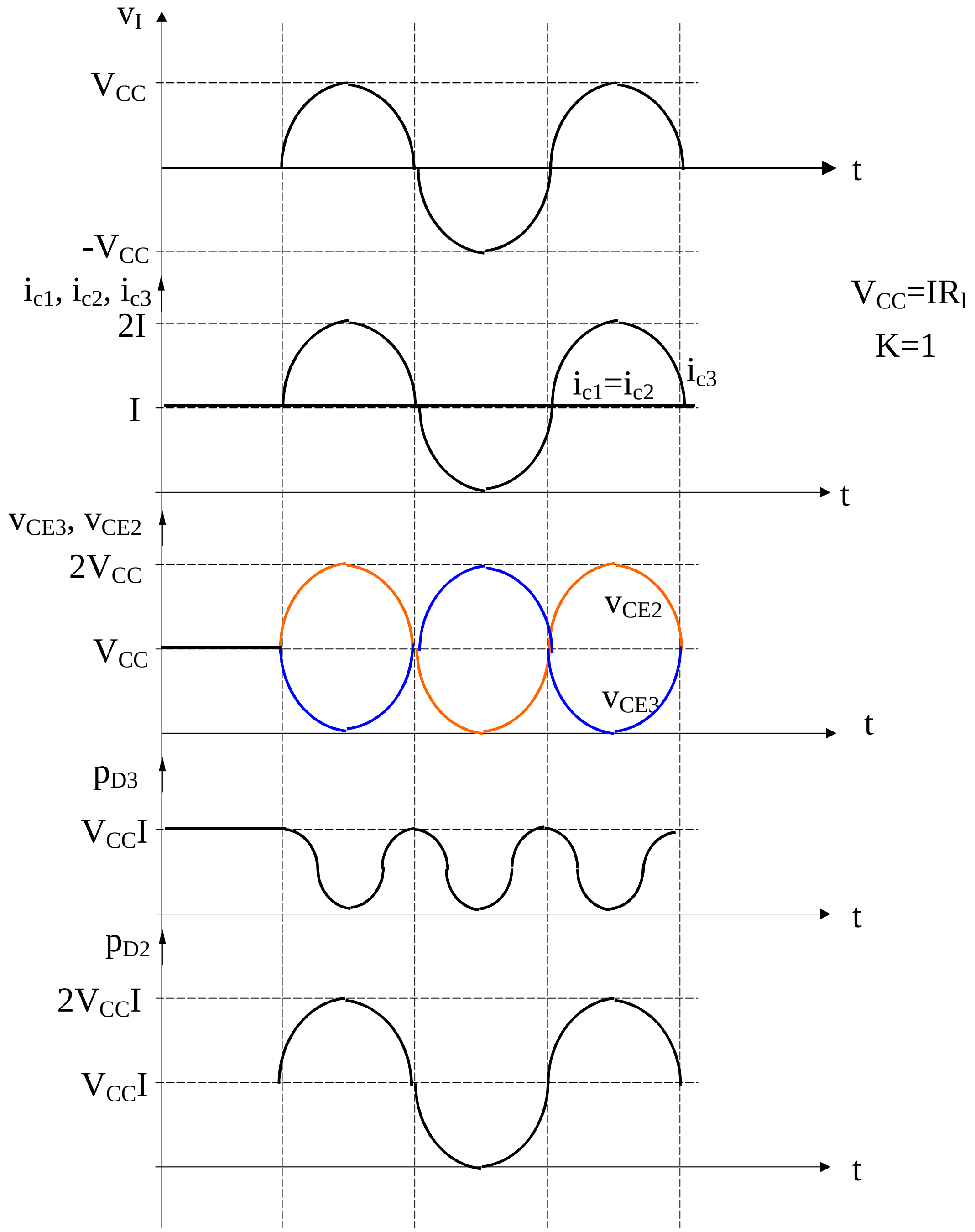
$$p_{D3} = v_{CE3} i_{C3} = \left(V_{CC} - \hat{V}_O \sin \omega t\right)\left(I + \hat{I}_O \sin \omega t\right)$$

$$p_{D3} = V_{CC} I (1 - K \sin \omega t)(1 + K \sin \omega t)$$

$$p_{D3} = V_{CC} I \left(1 - K^2 \sin^2 \omega t\right) = V_{CC} I \left(1 - \frac{K^2}{2} + \frac{K^2}{2} \cos 2\omega t\right)$$

Deci, puterea medie disipata pe tranzistorul Q_3 va fi:

$$P_{D3} = \frac{1}{2\pi} \int_0^{2\pi} p_{D3} d\omega t = V_{CC} I \left(1 - \frac{K^2}{2}\right)$$



vI
VCC
-VCC
t
ic1, ic2, ic3
2I
I
ic1=ic2
ic3
t
VCC=IRl
K=1
vCE3, vCE2
2VCC
VCC
vCE2
vCE3
t
pD3
VCCI
t
pD2
2VCCI
VCCI
t

Puterea disipata pe tranzistorul Q_2 este:

$$p_{D2} = i_{C2} v_{CE2} = I\left(V_{CC} + \hat{V}_O \sin \omega t\right) = I V_{CC}\left(1 + K \sin \omega t\right)$$

Deci, puterea medie disipata pe tranzistorul Q_2 va fi

$$P_{D2} = \frac{1}{2\pi}\int_0^{2\pi} p_{D2}\, d\omega t = V_{CC} I$$

Puterea consumata din sursele de alimentare va avea expresia:

$$p_A = V_{CC} i_{C3} + V_{CC} i_{C2} = V_{CC}\left(2I + KI \sin \omega t\right)$$

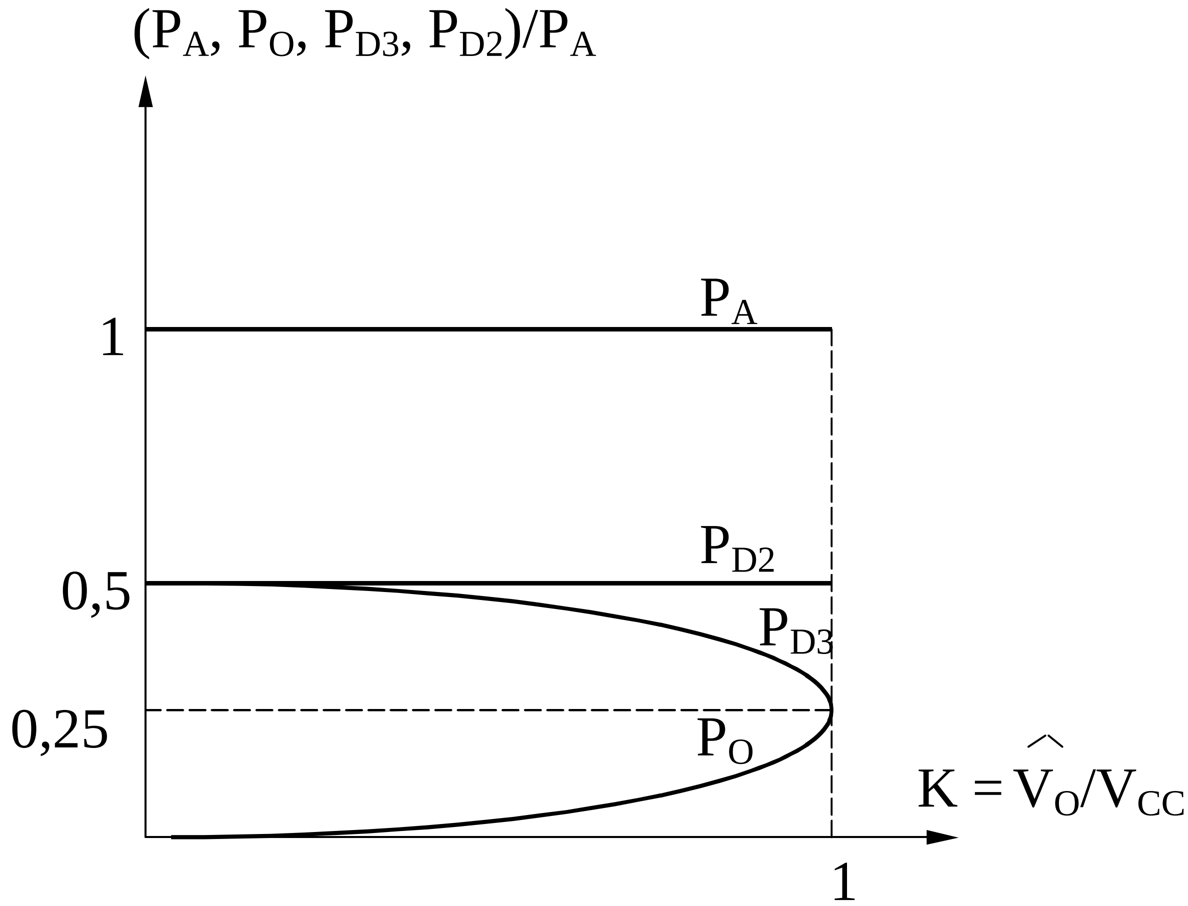
$$P_A = \frac{1}{2\pi}\int_0^{2\pi} p_A\, d\omega t = 2 V_{CC} I$$

Puterea medie la iesire este:

$$P_O = \frac{1}{2\pi}\int_0^{2\pi} p_O\, d\omega t = \frac{1}{2\pi}\int_0^{2\pi}\left(K V_{CC} \sin \omega t\right)\left(KI \sin \omega t\right) d\omega t = \frac{K^2 V_{CC} I}{2}$$

$$\eta_A = \frac{P_O}{P_A} = 25\% K^2$$

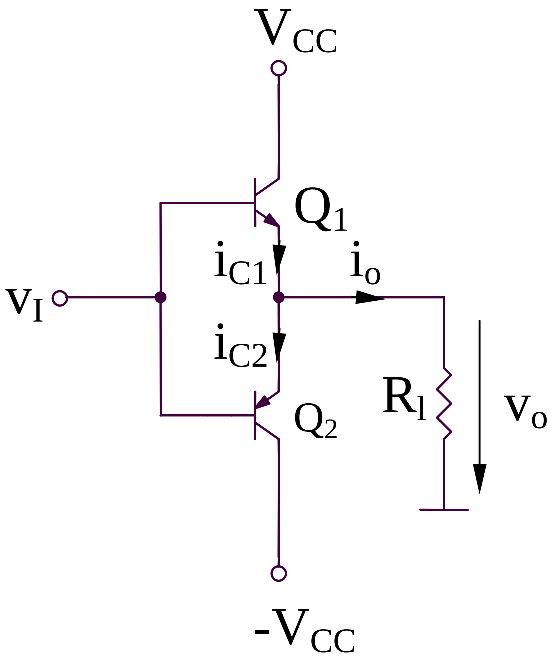
avand o valoare maxima de 25%.

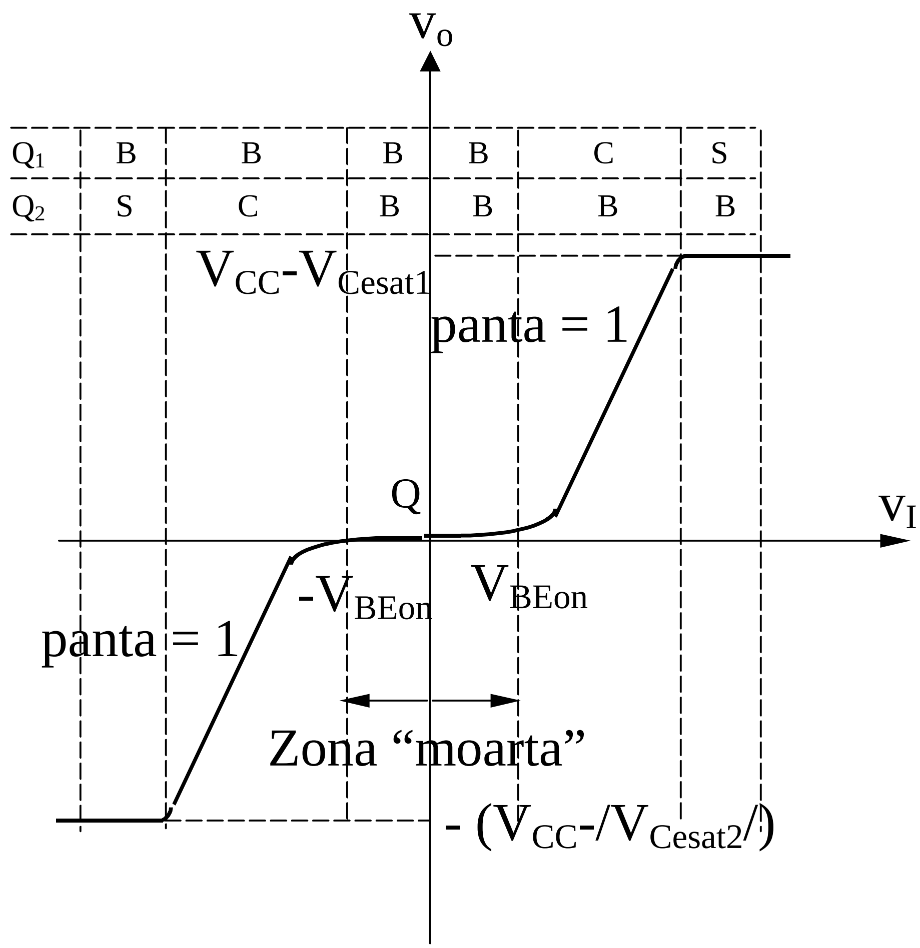


$$P_{D2} = P_{D3} + P_O$$

$$P_A = P_{D2} + P_{D3} + P_O = 2P_{D2}$$

5.3. Etajul de iesire elementar in clasa B



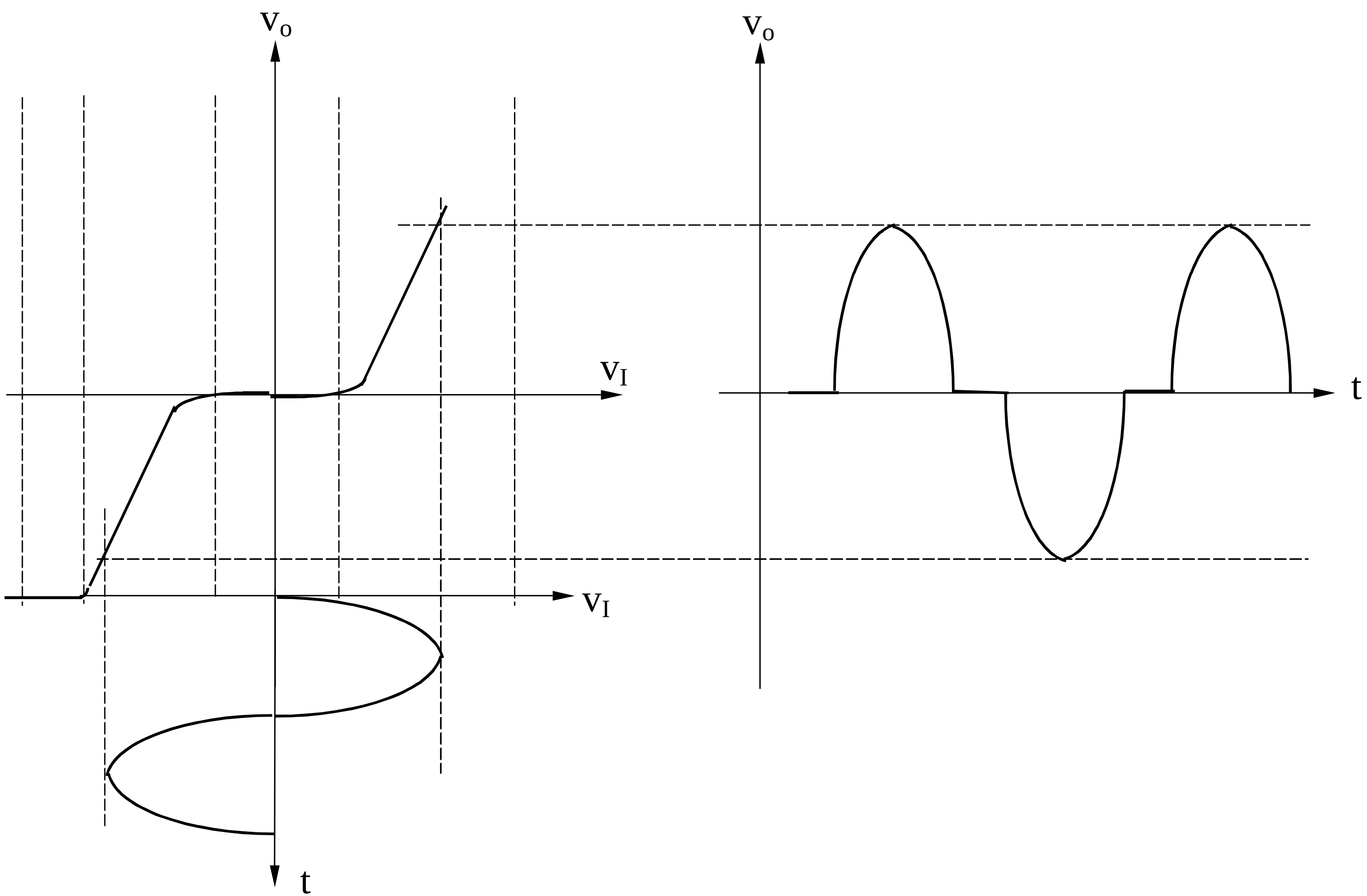


In repaus:

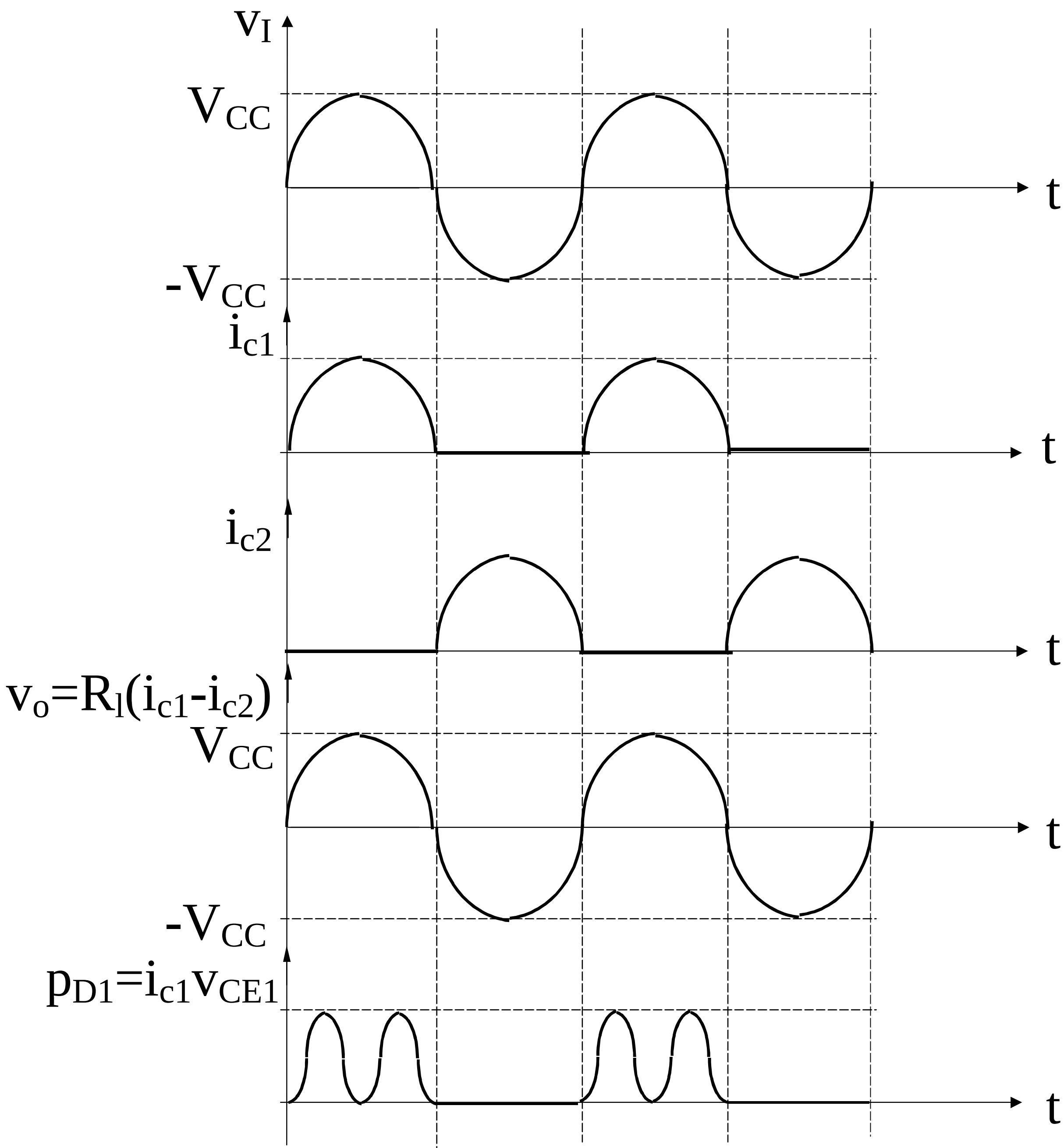
$$v_O = 0;\ i_O = 0;\ i_{c1} = i_{c2} = I;\ v_{BE1} + v_{EB2} = 0$$

Daca:

$$Q_1 \equiv Q_2;\ I_{S1} = I_{S2} = I_S \Rightarrow 2V_{th} \ln\left(\frac{I}{I_S} + 1\right) = 0 \Rightarrow I = 0 \Rightarrow i_{c1} = i_{c2} = 0$$



Caracteristica de transfer



v_I
V_{CC}
$-V_{CC}$
t
i_{c1}
t
i_{c2}
t
$v_o=R_l(i_{c1}-i_{c2})$
V_{CC}
$-V_{CC}$
t
$p_{D1}=i_{c1}v_{CE1}$
t

Dezavantajul major al etajelor de iesire in clasa B
- “zona moarta” (distorsiuni)

Solutie:
- utilizarea etajelor de iesire in clasa AB

Relatii energetice fundamentale

Notand:

$$\hat{V}_O = KV_{CC}$$

K fiind factorul de utilizare a tensiunii de alimentare, $0 \le K < 1$.
Puterea medie la iesire, P_O, este:

$$P_O = \frac{1}{2\pi}\int_0^{2\pi} p_O d\omega t = \frac{1}{2\pi}\int_0^{2\pi} \left(KV_{CC}\sin\omega t\right)\left(K\frac{V_{CC}}{R_l}\sin\omega t\right)d\omega t = \frac{K^2 V_{CC}^2}{2R_l}$$

Notand cu P_A puterea totala consumata de ambele surse de tensiune de alimentare:

$$P_A = 2V_{CC}I_{CC}$$

Componenta continua I_{CC} fiind:

$$I_{CC} = \frac{1}{2\pi}\int_0^{\pi} I_C \sin\omega t d\omega t = \frac{1}{\pi}\hat{I}_C = \frac{1}{\pi}\frac{\hat{V}_O}{R_l} = \frac{KV_{CC}}{\pi R_l}$$

se obtine:

$$P_A = K\frac{2V_{CC}^2}{\pi R_l}$$

Puterea disipata medie P_D pentru o pereche de tranzistoare in clasa B este:

$$P_D = P_A - P_O = \frac{V_{CC}^2}{2R_l}\left(\frac{4K}{\pi} - K^2\right)$$

Relatia anterioara reprezinta o parabola in K, al carei maxim se poate obtine prin anularea derivatei:

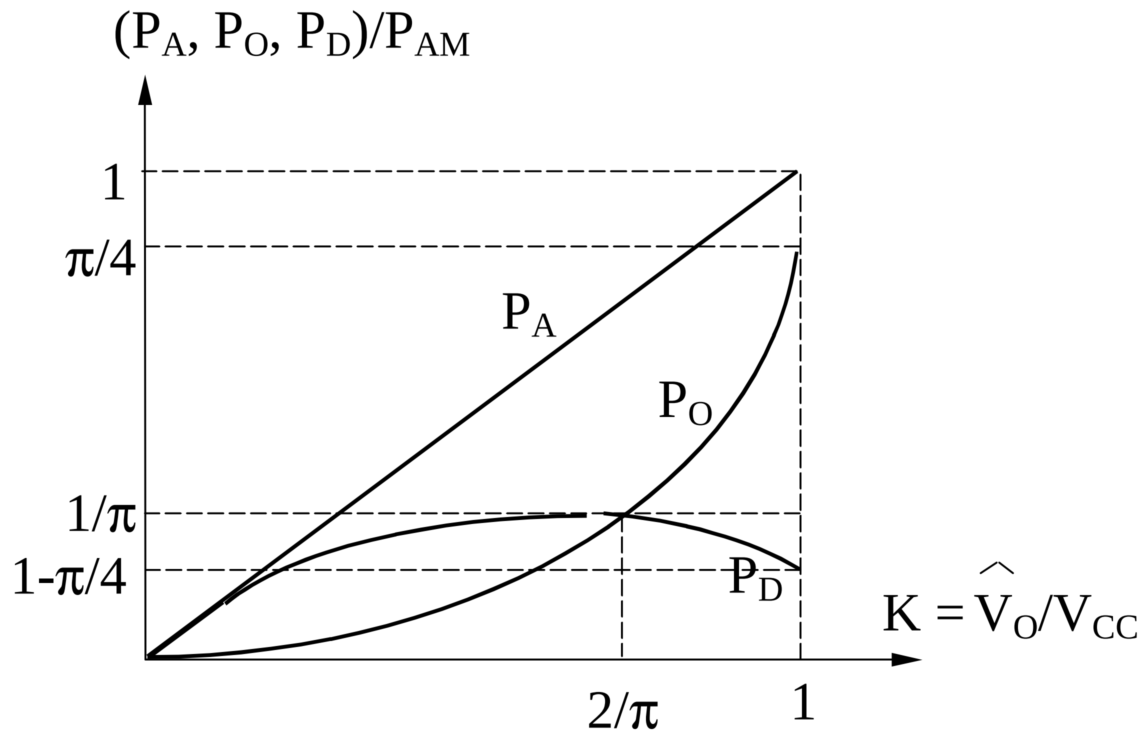
$$\frac{4}{\pi} - 2K = 0 \Rightarrow K = \frac{2}{\pi}$$

Pentru aceasta valoare a lui K se va obtine maximul puterii medii disipate (pentru amandoua tranzistoarele):

$$P_{DM} = \frac{2}{\pi^2}\frac{V_{CC}^2}{R_l} = \frac{4}{\pi^2}\frac{V_{CC}^2}{2R_l} = \frac{4}{\pi^2}P_{OM} \qquad P_{OM} = \frac{V_{CC}^2}{2R_l}$$

Pe graficele urmatoare sunt reprezentate puterile normate in functie de K:

$$\frac{P_A}{P_{AM}} = K; \qquad \frac{P_O}{P_{AM}} = \frac{\pi K^2}{4}; \qquad \frac{P_D}{P_{AM}} = K\left(1 - \frac{K\pi}{4}\right)$$

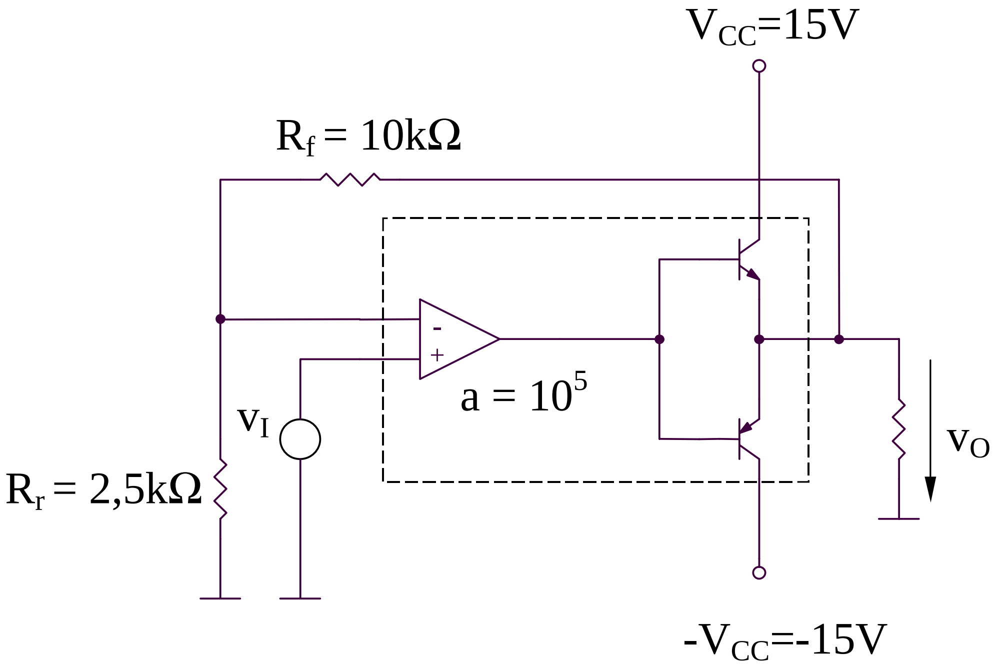


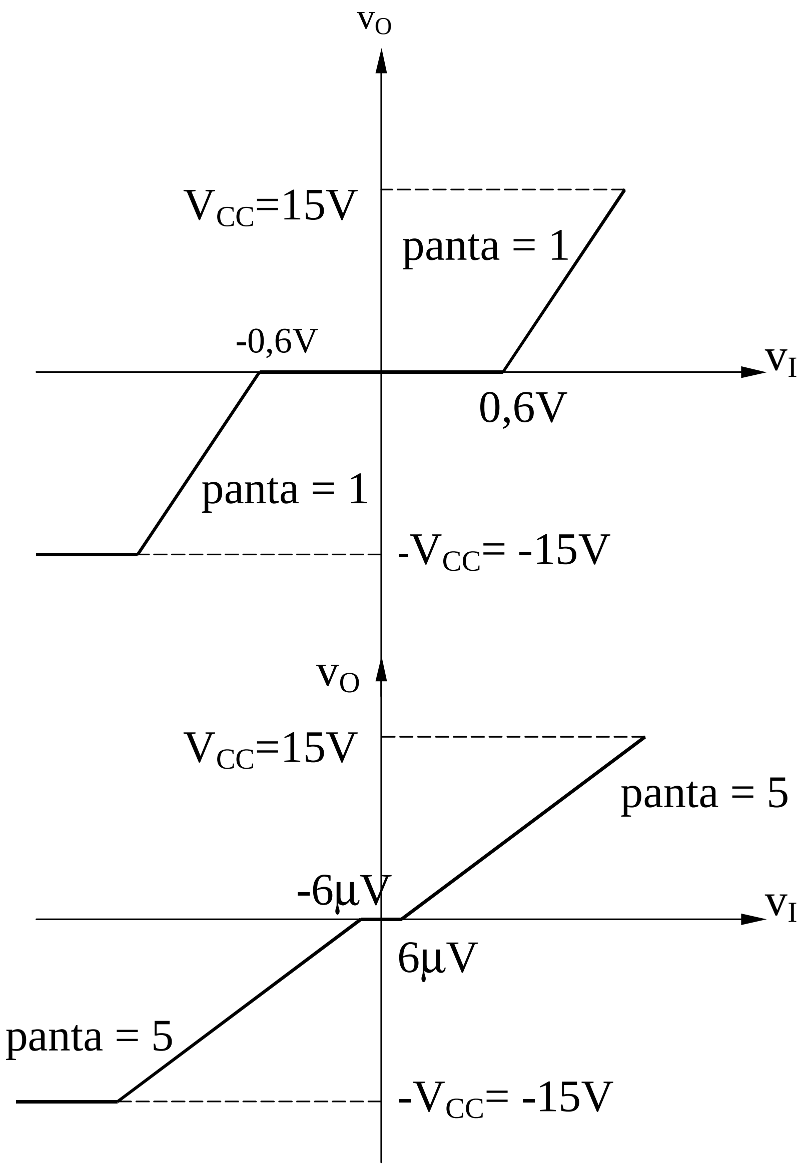
Randamentul etajului este:

$$\eta = \frac{P_O}{P_A} = K\frac{\pi}{4}$$

Valoarea sa maxima se obtine pentru K=1 si este π/4 (78.5%).

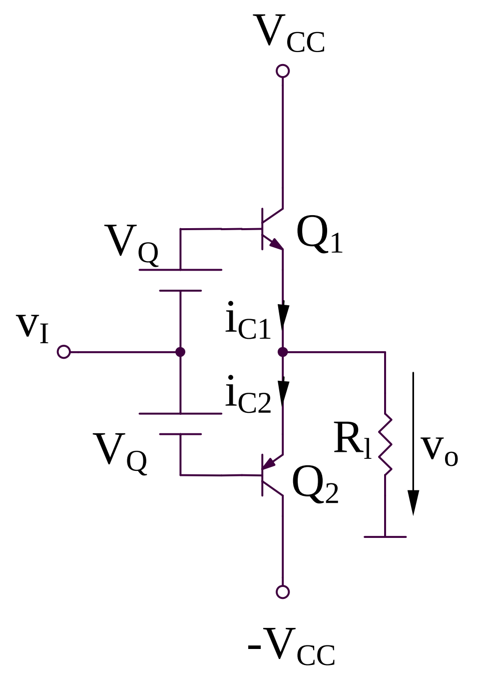
5.4. Reducerea neliniaritatii etajului de iesire in clasa B prin utilizarea rectiei negative





5.5. Etajul de iesire in clasa AB

5.5. Etajul de iesire in clasa AB

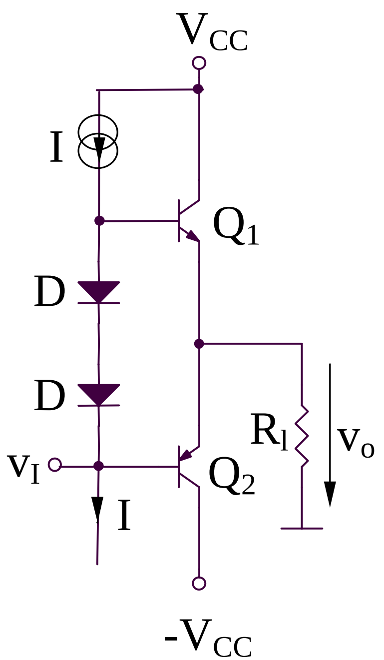


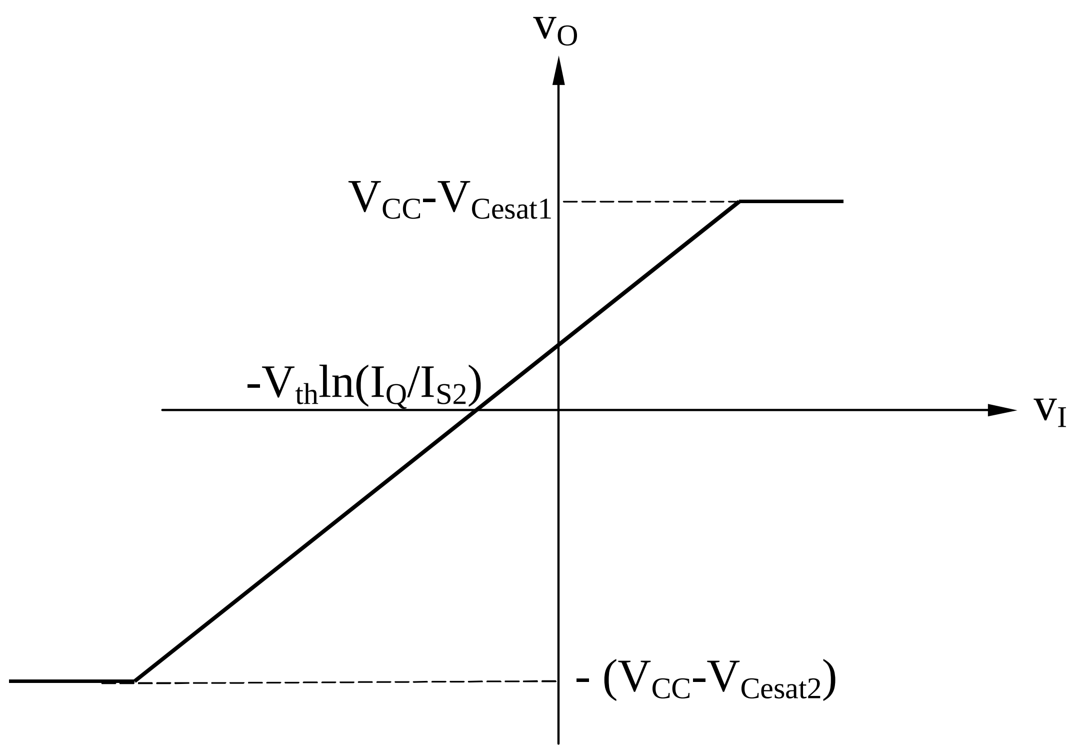
Pentru obtinerea unei bune liniaritati a functiei de transfer, este necesar:

- sa existe o imperechere cat mai buna intre parametrii tranzistoarelor complementare
- sa se realizeze o pre-polarizare corespunzatoare a etajului de iesire in repaus
- pre-polarizarea implementata sa asigure evitarea ambalarii termice a etajului

Circuit pentru evitarea ambalarii termice a etajului de iesire (1)

Tensiunea care asigura pre-polarizarea etajului de iesire trebuie sa prezinte o variatie particulara cu temperatura (de exemplu, o tensiune baza-emitor)



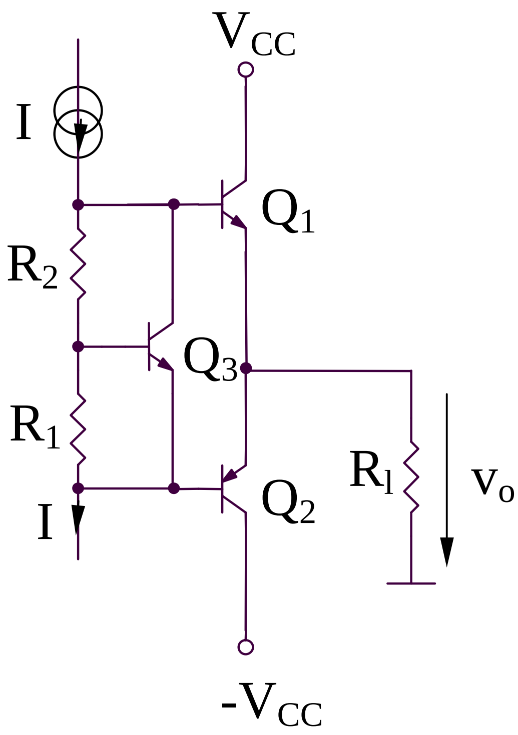


Tranzistoarele conectate ca diode trebuie sa prezinte o dependenta de temperatura similara cu cea a tranzistoarelor finale. In repaus:

$$v_O = 0$$

$$V_{BE1} + V_{EB2} = 2V_D \Rightarrow V_{th} \ln\left(\frac{I_Q}{I_{S1}}\frac{I_Q}{I_{S2}}\right) = 2V_{th} \ln\left(\frac{I}{I_{SD}}\right) \Rightarrow I_Q = I\,\frac{\sqrt{I_{S1} I_{S2}}}{I_{SD}}$$

Circuit pentru evitarea ambalarii termice a etajului de iesire (2)

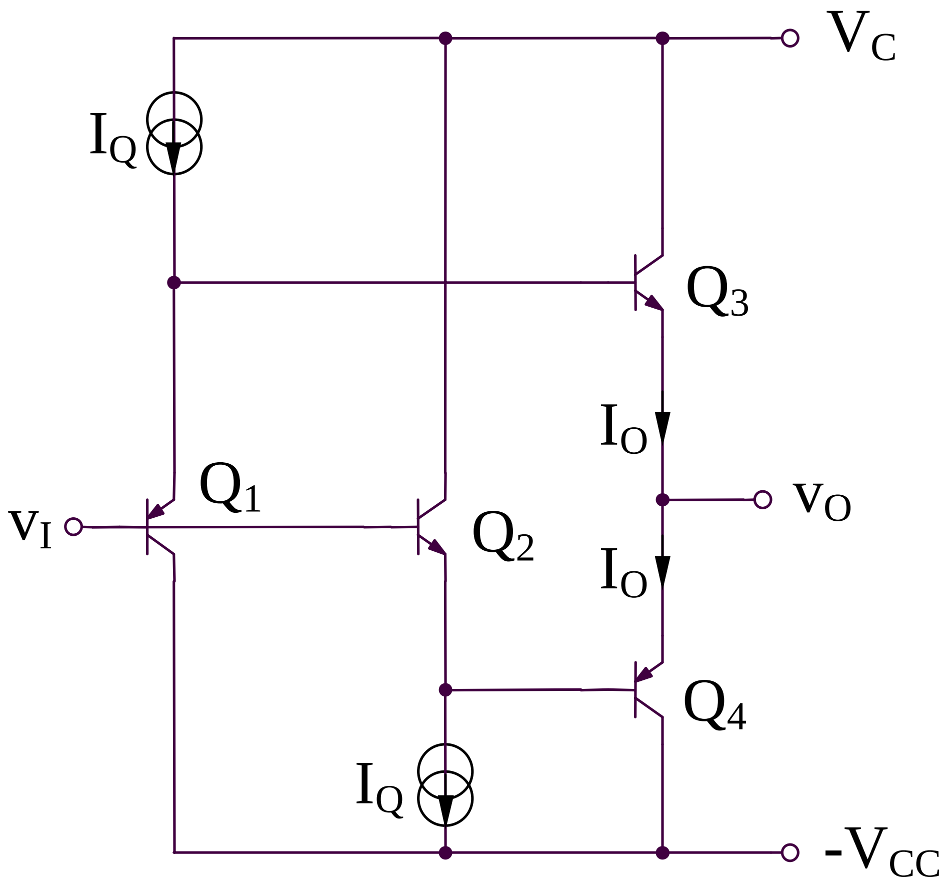


$$\left.\begin{aligned} v_{BE1} + v_{EB2} &= v_{CE3} \\ v_{CE3} &= \frac{v_{BE3}}{R_1}\left(R_1 + R_2\right) \end{aligned}\right\} \Rightarrow$$

$$\Rightarrow V_{th}\left(\ln\frac{I_Q}{I_{S1}} + \ln\frac{I_Q}{I_{S2}}\right) = \left(1 + \frac{R_2}{R_1}\right) V_{th} \ln\frac{I}{I_{S3}}$$

$$\Rightarrow I_Q = \sqrt{I_{S1} I_{S2} \left(\frac{I}{I_{S3}}\right)^{1+\frac{R_2}{R_1}}}$$

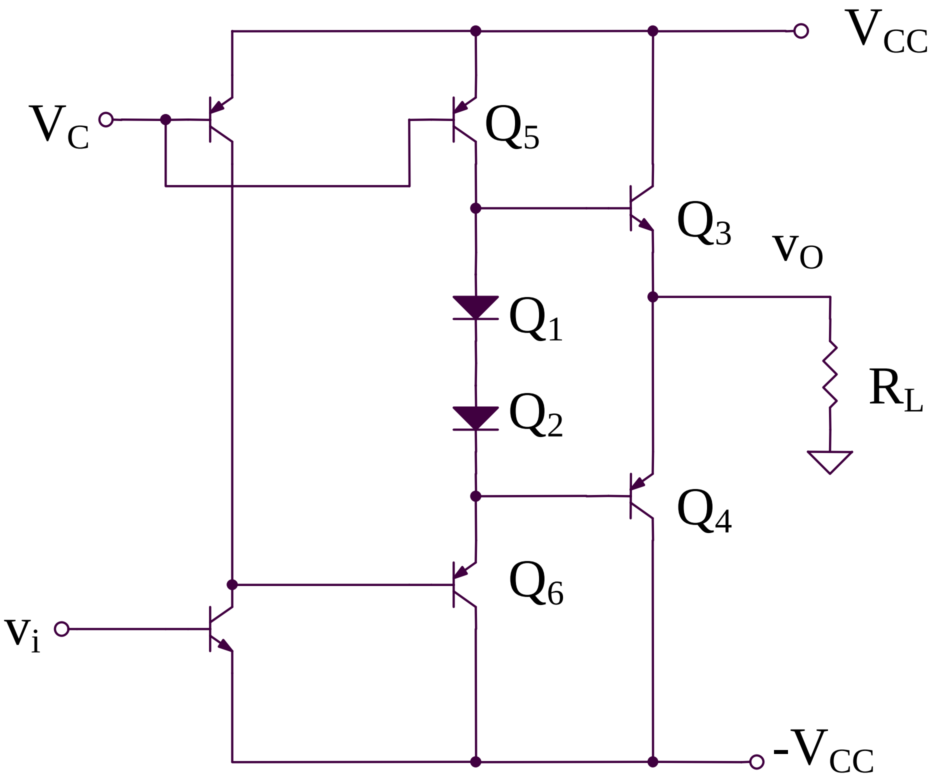
Circuit pentru evitarea ambalarii termice a etajului de iesire (3)



$$/V_{BE1}/ + V_{BE2} = V_{BE3} + /V_{BE4}/$$

$$2V_{th} \ln \frac{I_Q}{I_S} = 2V_{th} \ln \frac{I_O}{I_S} \Rightarrow I_O = I_Q$$

Circuit pentru evitarea ambalarii termice a etajului de iesire (4)



$$V_{BE1} + V_{BE2} = V_{BE3} + V_{EB4}$$

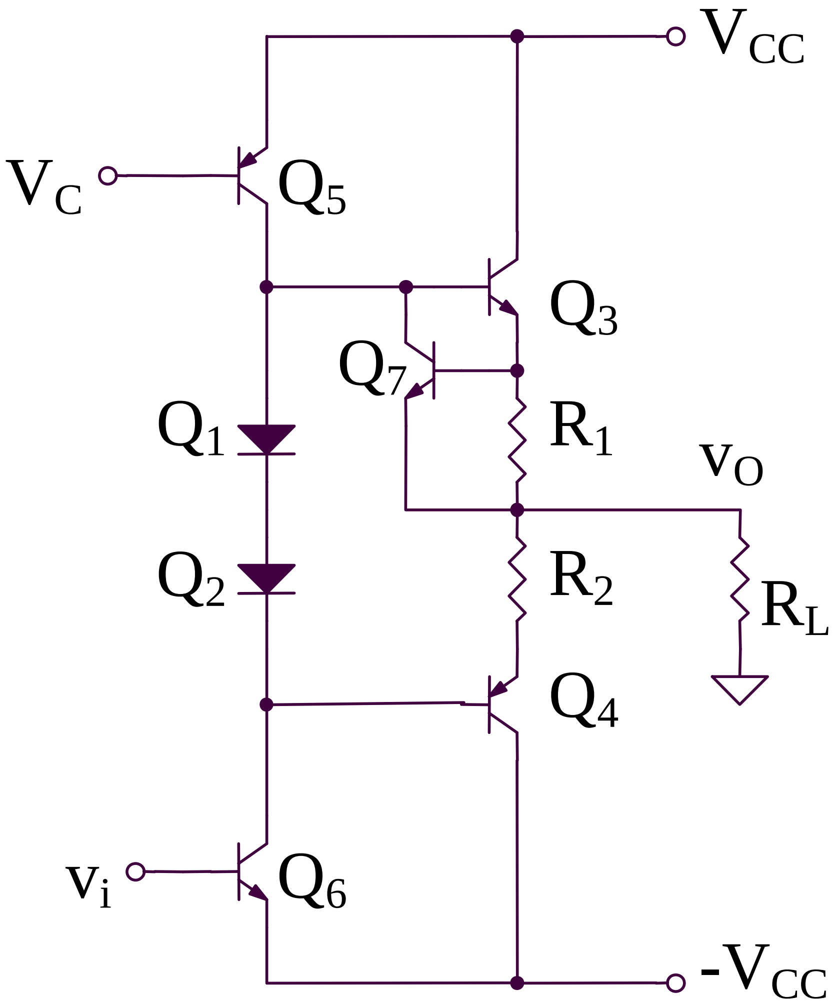
$$V_{th} \ln \frac{I_{C1}}{I_{S1}} + V_{th} \ln \frac{I_{C2}}{I_{S2}} = V_{th} \ln \frac{I_{C3}}{I_{S3}} + V_{th} \ln \frac{I_{C4}}{I_{S4}}$$

$$\Rightarrow I_{C3} = I_{C4} = I_{C1} \sqrt{\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}}$$

$$V_{O\,max}^{+} = V_{CC} - V_{EC5sat} - V_{BE3}$$

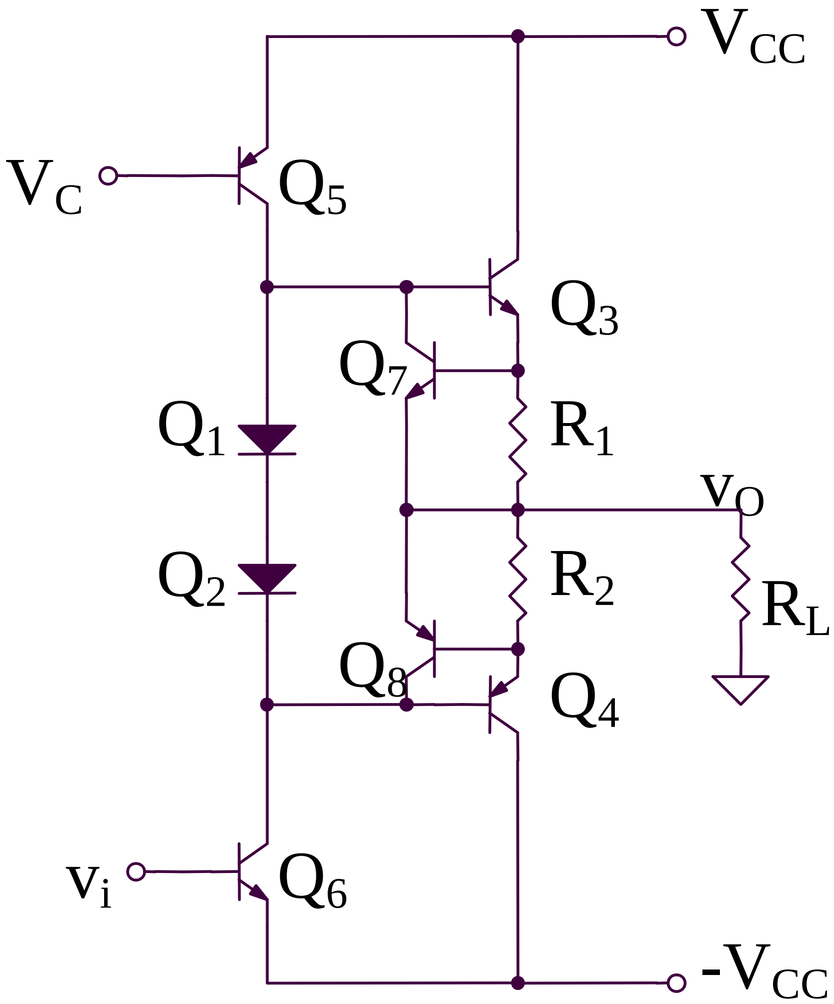
$$V_{O\,max}^{-} = -V_{CC} + V_{EC6sat} + V_{EB4}$$

Circuit pentru protectia la suprasarcina (1)



$$I^{+}_{O\,max} = \frac{V_{BE7}}{R_1}$$

Circuit pentru protectia la suprasarcina (2)



$$I_{O\,max}^{+} = \frac{V_{BE7}}{R_1}$$

$$I_{O\,max}^{-} = \frac{V_{EB8}}{R_2}$$