Vivado
New Project Tutorial

This tutorial guides you through the typical steps of design, simulation, synthesis and implementation of a simple project, designed from scratch, like those that you will do at the Applications for the Digital Integrated Circuits course.

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Project File Management

The FPGA design flow goes through the stages shown in Figure 1. The Vivado software arranges these stages in the *Flow Navigator* and guides you through it.

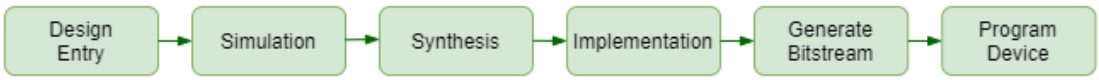

Figure 1: FPGA design flow

Various files are employed in each design flow stage, all of them created and managed by Vivado, except for the source files, that are written by you, the designer. All files created by Vivado reside in the project folder (directory) and its subfolders. Your source files should also reside inside the project folder.

To keep things as neat as possible, strictly follow these two rules:

- **Each project has its own folder.**
- **All (Verilog) source files are saved in their default locations.**

The project folder has the structure shown in Figure 2.

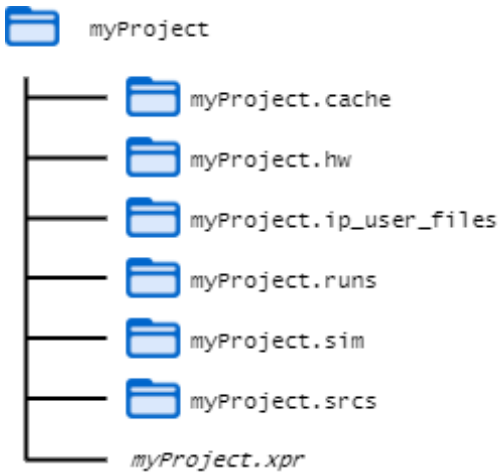

Figure 2: Vivado project folder structure.

Some folders are created by Vivado at the project creation, others are created during later stages of the FPGA design flow. Most of the files are taken care of by Vivado, so you need not bother about their names or where they are located. The only files you should care about are:

- design source files
- simulation source files
- constraints file

Remember:

- **All project source files should reside inside the project folder.**

Create a New Project

Open the Vivado program. Wait a couple seconds until Vivado opens the Start Page.

From the Start Page open the New Project wizard by clicking on **Create Project** option in the **Quick Start** panel (Figure 3). Alternatively you may open the New Project wizard from Vivado's main menu, selecting **File** -> **New Project …** .

Figure 3: Quick Start panel from Vivado Start Page

The New Project wizard opens a dialog with a brief description of the wizard (Figure 4). Click **Next** to advance through the New Project wizard steps.

Figure 4: New Project wizard open dialog

In step 1 (Project Name) of the New Project wizard (Figure 5) set the name of the project in the Project Name text editor field. The default name is project_1, but you should change it to a more descriptive name. Vivado uses this name as a prefix for the names of the project's subfolders.

Check the box Create project subdirectory. You may keep the default Project Location (`/home/student` on Linux) or change it to a convenient location but be sure to create a project subdirectory such that all project files are kept in its subdirectory and not mixed with other files, unrelated to this project.

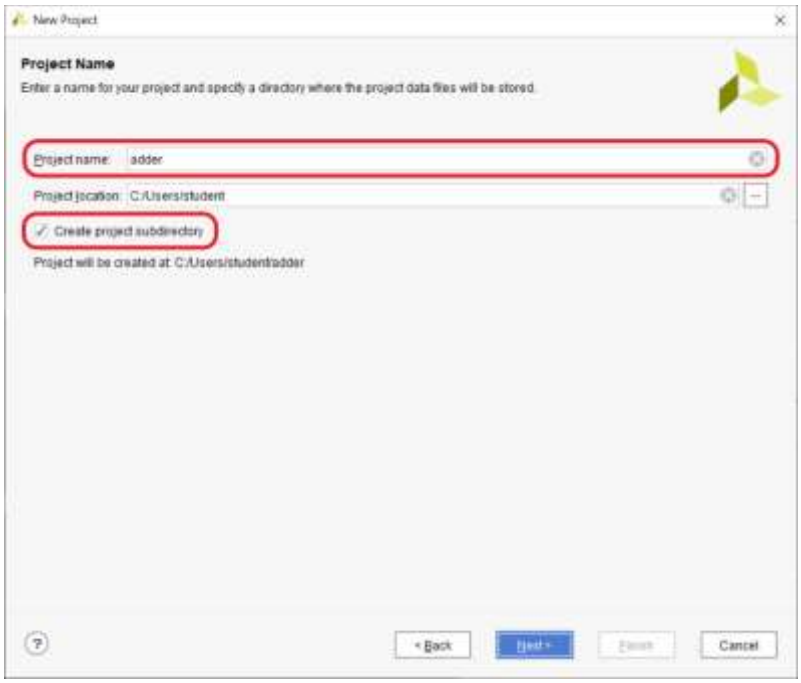

Figure 5: New Project wizard step 1 (Project Name)

Click **Next** to continue.

In step 2 (Project Type) keep the default selection *RTL Project*. Click **Next** to continue.

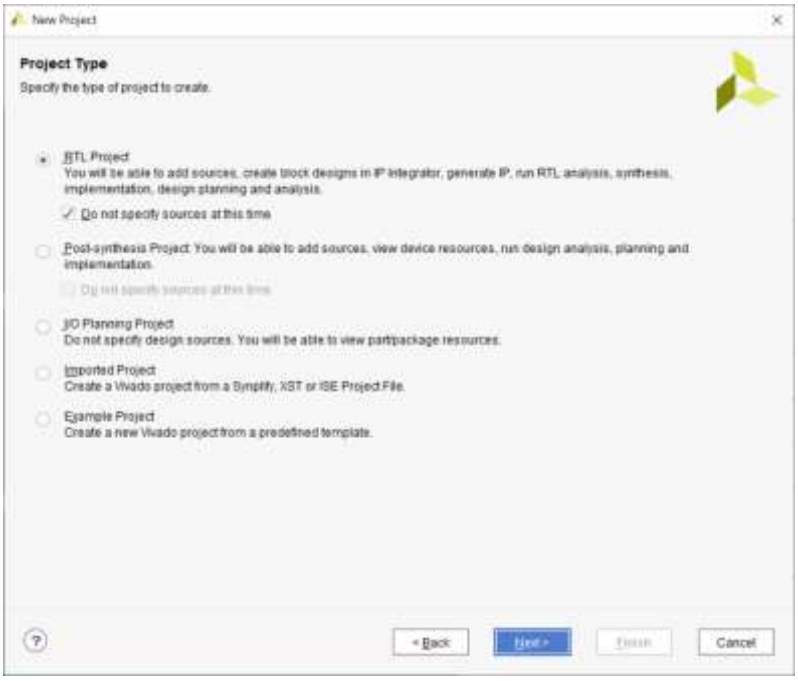

Figure 6: New Project wizard step 2 (Project Type)

In step 3 [Default Part] of the New Project wizard change the tab from **Parts** to **Boards**

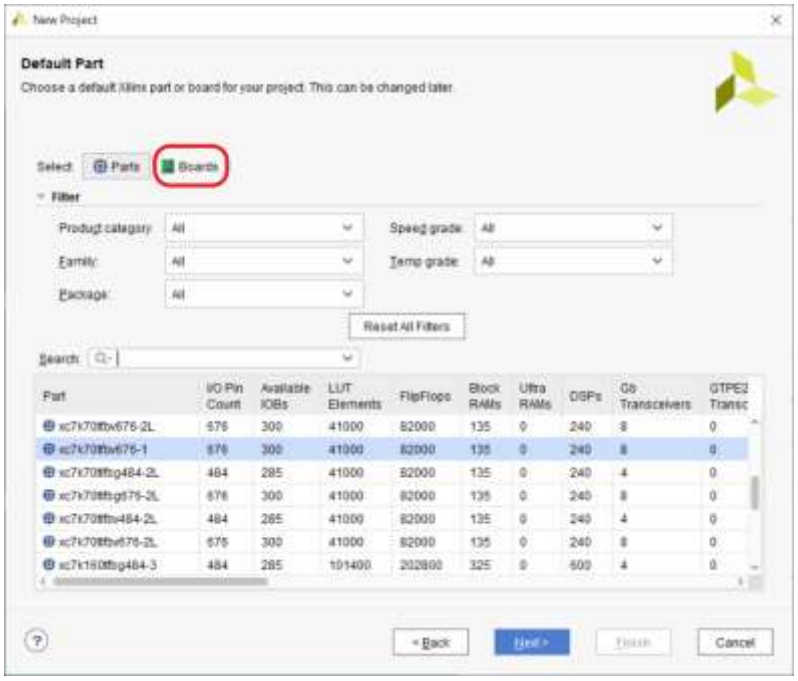

Figure 7: New Project wizard step 3 (Default Part)

Select the pynq-z2 board from the list (Figure 8).

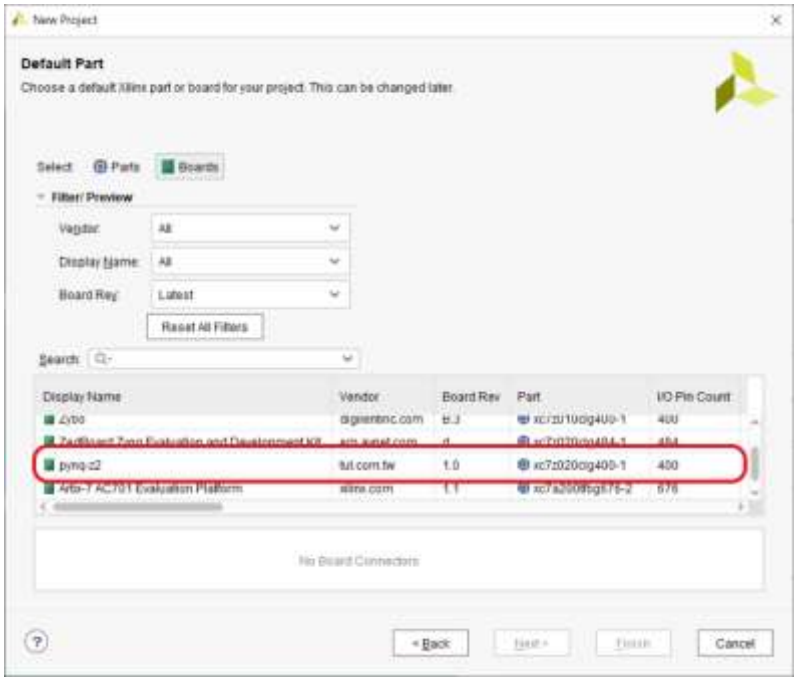

Figure 8: New Project wizard step 3 (Default Part) board selection

After you selected the board (Figure 9) click **Next**.

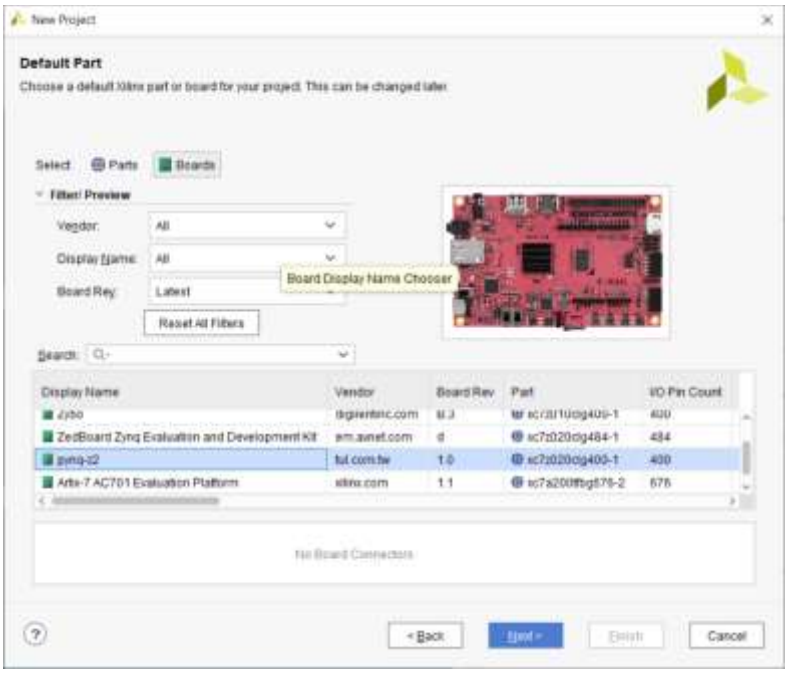

Figure 9: New Project wizard step 3 (Default Part) with the Pynq-Z2 board selected

The last dialog of the New Project wizard (Figure 10) shows a brief description of the settings and selections you have made. Click **Finish**.

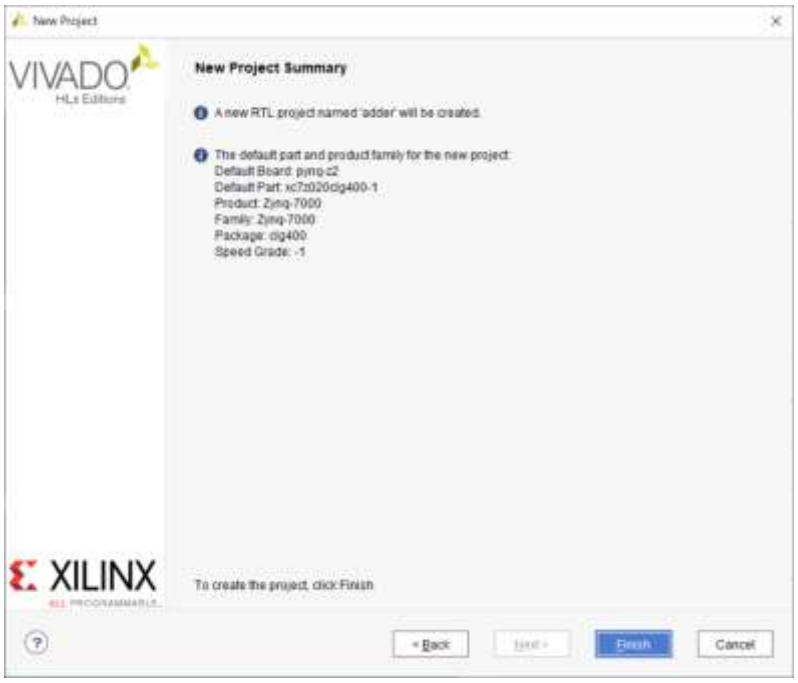

Figure 10: New Project wizard summary

After Vivado creates and initializes the project, it opens the Project Manager window.

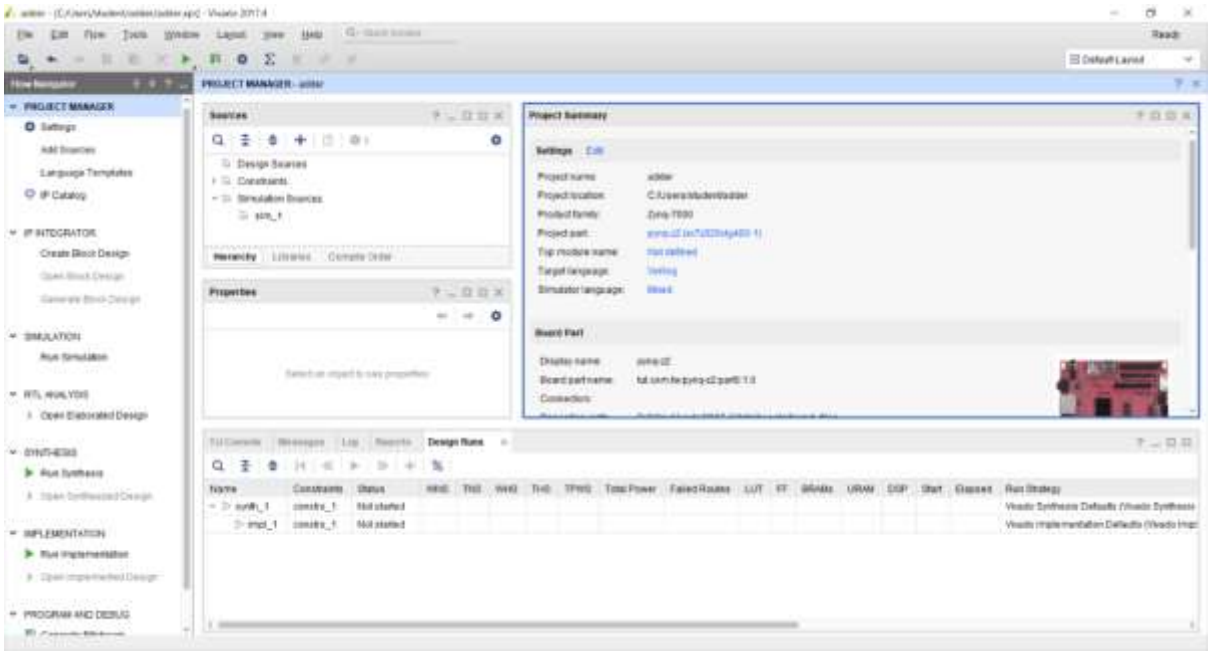

Figure 11: Vivado project manager window

Create Source Files

To create a new design source file, click on the Plus button in the Sources panel (Figure 12) from the project manager window.

Figure 12: Open a new source file

In the Add Sources window that opens (Figure 13), select and click **Next**.

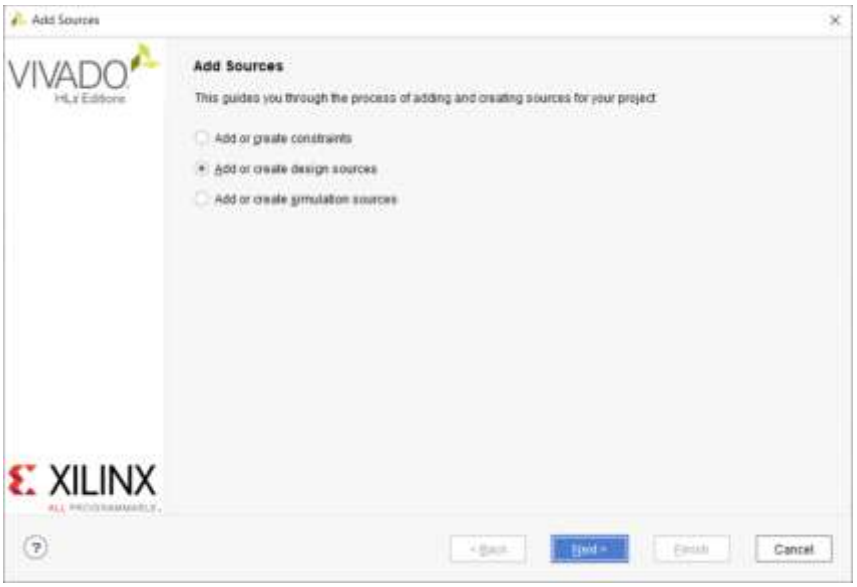

Figure 13: Source file type selection

Alternatively, in the Sources panel you may right click on the desired type you want to create (Design Sources, Constraints or Simulation Sources) and from the pop-up menu select the Add Sources … option (Figure 14).

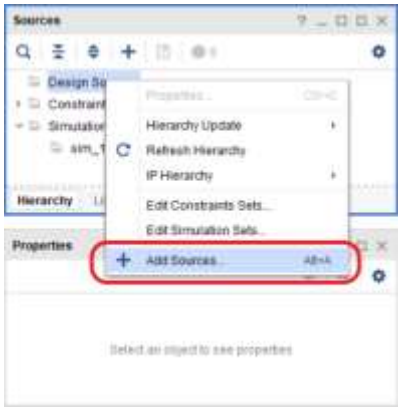

Figure 14: Open a new source file of the desired type

This alternative way opens the Add Souces dialog with the desired file type selected by default.

Click **Next**.

The Add Sources dialog opens (Figure 15). You may add files to the project or create new ones. Click on **Create File** button.

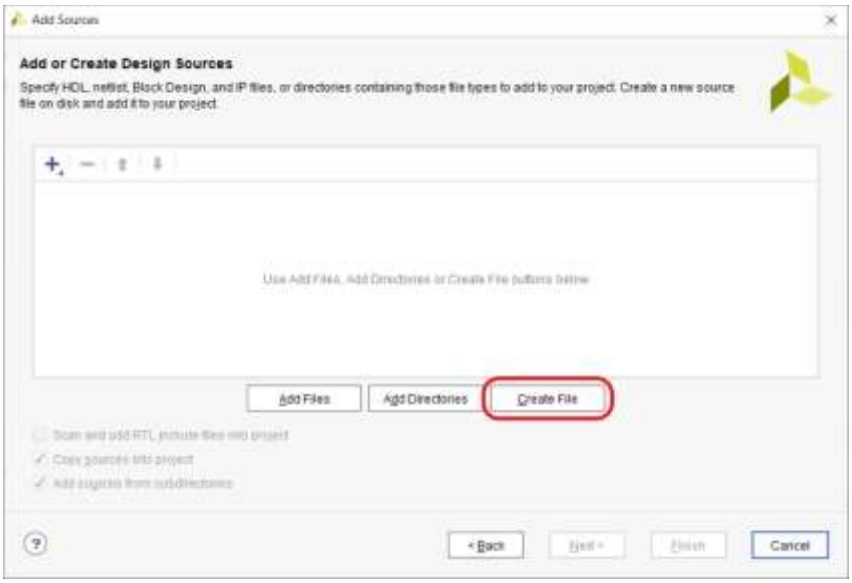

Figure 15: Add Sources window

In the small dialog box that opens (Figure 16) enter the desired name for the source file in *File Name* text editor field but keep unchanged the default values for *File Type* and *File Location*. Click **OK**.

Figure 16: Enter the new file name

The new file is added to the list of files of your project (Figure 17).

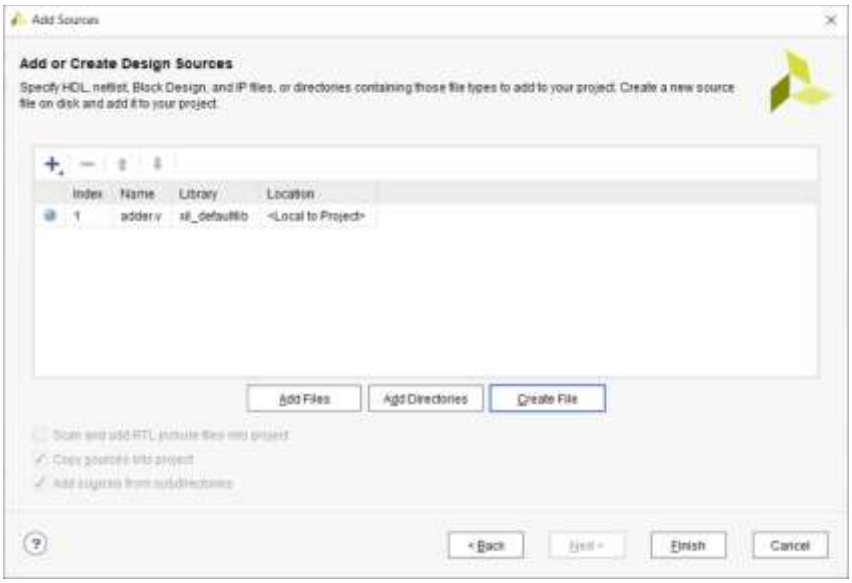

Figure 17: Add Sources window with the new file added to the list

After you added and created the desired files click **Finish**.

Immediately after that Vivado opens another dialog (Figure 18) that allows you to define the interface for each newly created Design Source and Simulation Source. You may skip these option.

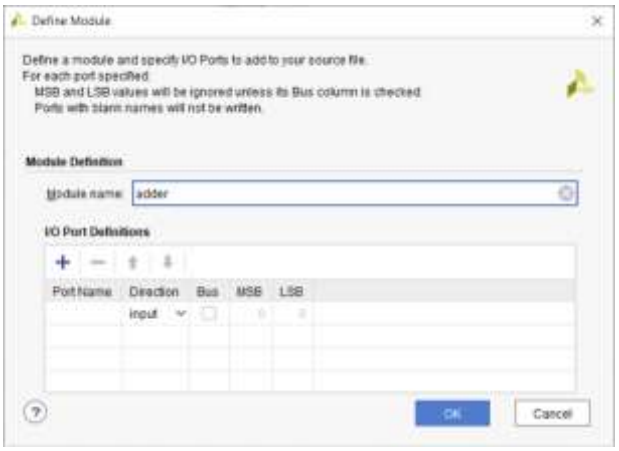

Figure 18: Define Module window

The interface of a module may be edited in the I/O Port Definitions table. For a single bit port you should enter a Port Name and select its Direction (input by default). As an example, a newly created adder module is defined with 2 one-bit inputs a and b, and a third port, c, is declared as output. To change the Direction click on the downward arrow and select the desired direction from the drop-down list.

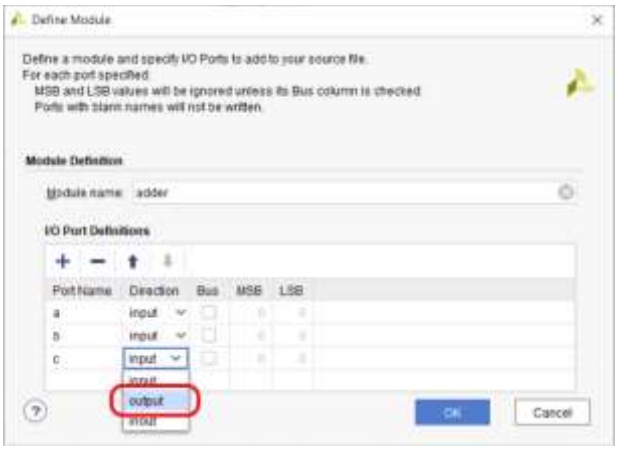

Figure 19: Define module window, change a port direction

Some ports may have more than one bit. They may be thus defined by checking the Bus checkbox and entering the MSB and LSB values. LSB should be 0. MSB is equal to the desired width minus 1. The MSB and LSB values (default value is 0) may be changed by editing the MSB and LSB textbox or using the up and down arrows to increment or decrement the value.

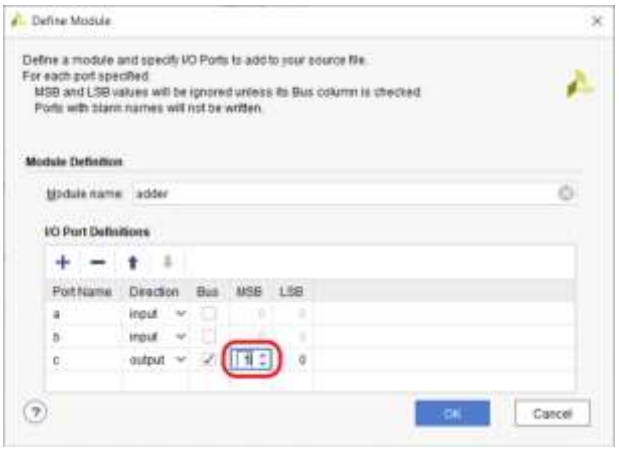

Figure 20: Define module window, change a port width

Click **OK**. To finish file creation.

- **Each module is in a separate source file.**
- **The name of the source file is the name of the module.**
- **Keep for any created file the default location.**
- **The top-level module name and its source file name must match the name of the project.**

Add Source Files

If you want to include in your project a file that is already on your computer open the Add Sources window as shown in the previous section and click **Add Files** button (Figure 21):

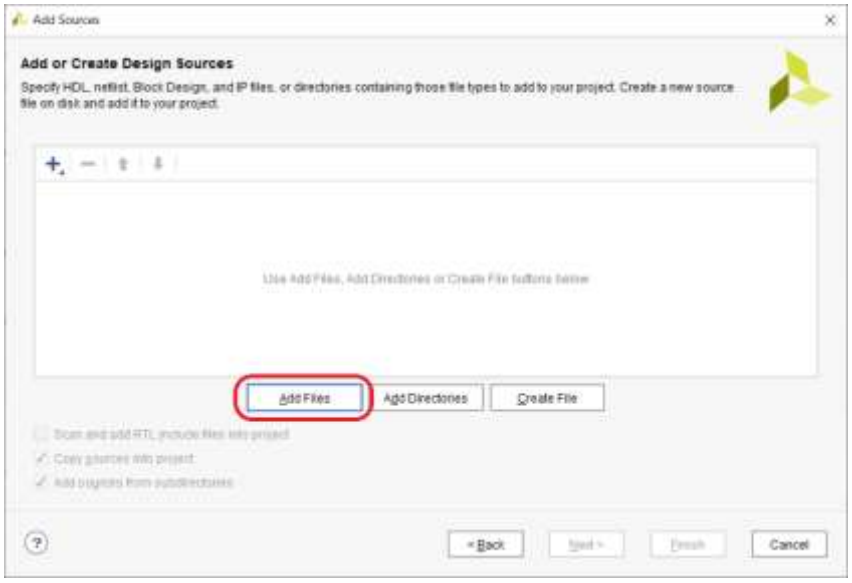

Figure 21: Add Sources window.

A file browser opens (Figure 22). Use the Up button (encircled in red) to go up in the file hierarchy and click on folder names in the left panel to go down in the file hierarchy. Select the files you want to copy into the project and click **OK**.

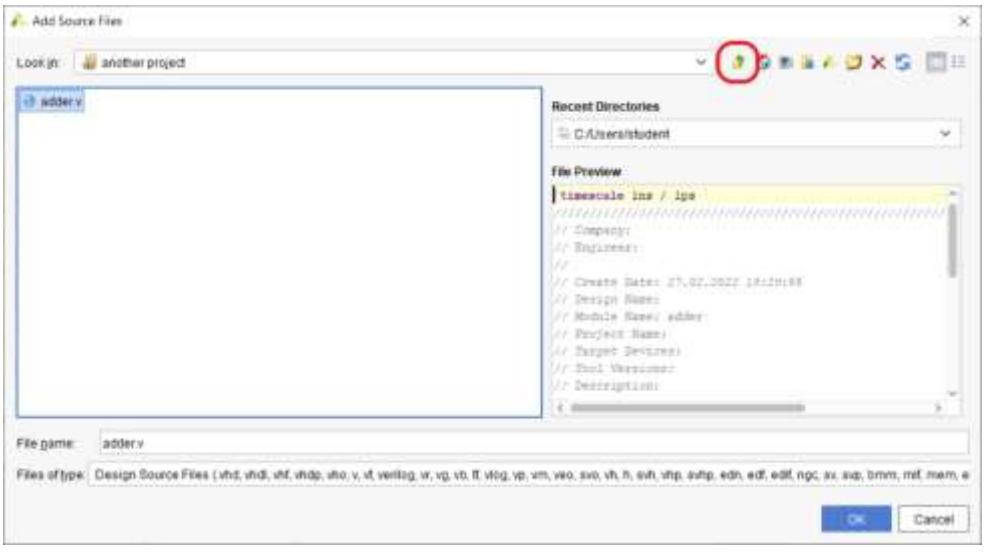

Figure 22: Add Source File browser

The selected files are added to the list of project files in the Add Sources window (Figure 23). You should check the *Copy sources into project* checkbox. Click **Finish**.

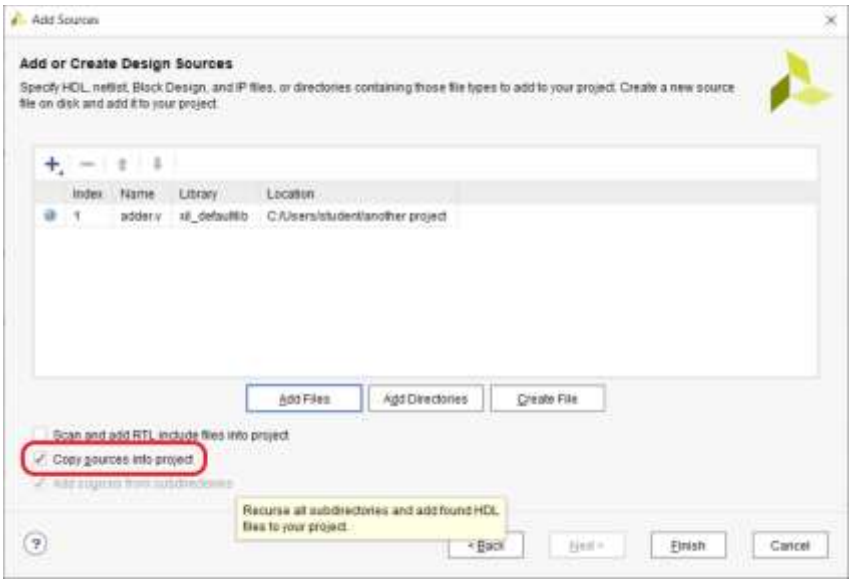

Figure 23: Add Sources window

- **Make sure that any added file is also copied into project.**

Source File Editor

To open a file for editing double click the file in the *Sources* panel. The editor window (Figure 24) opens in another tab of the rightmost panel of the Vivado Project window. You may edit all the file.

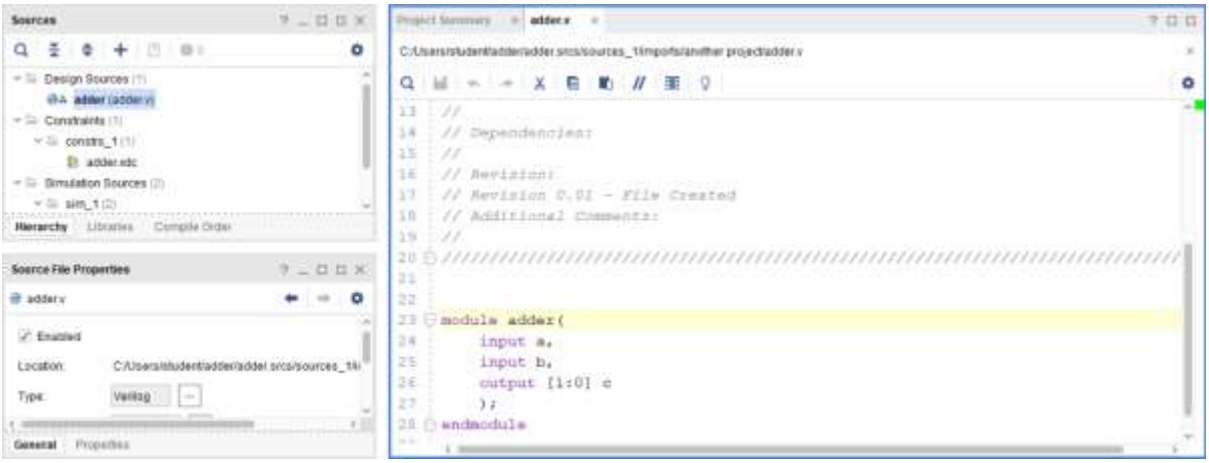

Figure 24: File editor window

To save the file click on the Save icon at the top row of the editor window. After a file is changed and saved Vivado updates the hierarchy of modules.

Simulation

On the left panel Flow Navigator expand the Simulation section and click on **Run Simulation**. From the pop-up menu list select **Run Behavioral Simulation**. Vivado starts the elaboration of the design. This takes some time while a dialog shows the progress of this compilation.

If the elaboration succeds, Vivado opens the Simulation window (Figure 25).

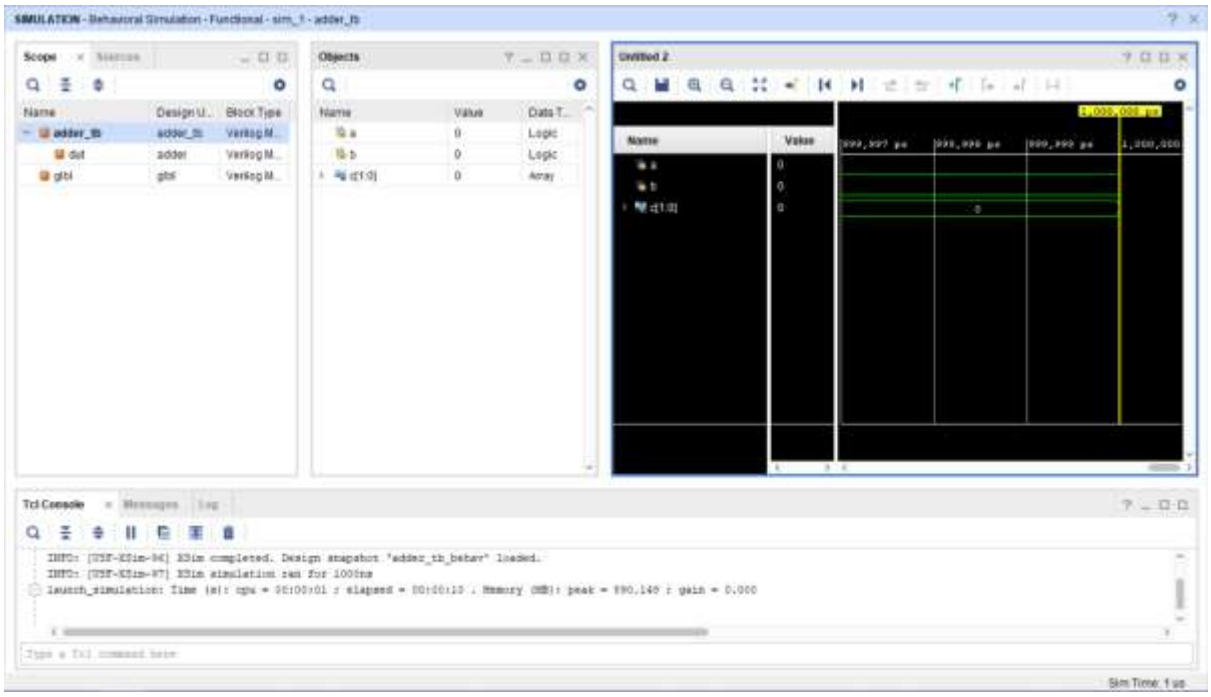

Figure 25: Vivado Simulation window

The Simulation window has four panels. The leftmost Scope panel shows the hierarchy of the modules instantiated in your project, with the testbench module at the root of the hierarchy. The middle Objects panel lists all signals of the module that is selected in the Scope hierarchy. The rightmost panel draws the waveforms of the signals chosen to be displayed. By default the Simulation window opens with the testbench module selected and with all its signals been displayed on the waveform panel.

The bottom panel reports messages from Vivado and logs everything displayed by the simulated modules themselves.

The most important controls of the simulation are the Restart, Run All and Relaunch Simulation. They are available from Vivado main menu Run section, but are easier to choose from Vivado toolbar (Figure 26).

Figure 26: Vivado Simulation controls

The Wave window may be arranged to suit your needs. You may rearrange the signals by clicking a signal name and dragging it up or down in the list. You may shrink or expand the time scale using the Zoom In, Zoom Out and Zoom Fit icons of the Wave window's toolbar (Figure 27).

Figure 27: Wave window main controls

Note: If there are no signals in the Wave and Object windows, that means the testbench has not compiled because of compiling errors, or it has not loaded because the module it instantiates does not match the compiled top-level design module. In the Browser panel at the left of the simulator window you will see some instances, but not the testbench instance. In that case you must look for the errors in the Transcript panel at the bottom of the simulation window, close the simulator, fix the errors in the testbench and then relaunch the simulator.

I/O Ports Assignment

Synthesis and Implementation

Device Programming

Quick Project Guide

- **New Project** wizard
  - Step 1 [Project Name]
    - **Project name**: *myProject*
    - Check *Create project subdirectory* checkbox
  - Step 2 [Project Type]
    - Select *RTL Project*
  - Step 3 [Default Part]
    - Change tab to **Boards**
    - From Boards list select the *pynq-z2* board
- Create source files
  - **Add Sources** wizard
  - Select
  - Edit & Save
- *Flow Navigator* -> SIMULATION -> *Run Simulation* -> **Run Behavioral Simulation**
  - Analyse, debug, edit, recompile, restart, run
- *Flow Navigator* -> SYNTHESIS -> **Run Synthesis**
- *Flow Navigator* -> IMPLEMENTATION -> **Run Implementation**
- *Flow Navigator* -> PROGRAM AND DEBUG -> **Generate Bitstream**
- *Flow Navigator* -> PROGRAM AND DEBUG -> Open Hardware Manager -> **Program device**
  - Power on the physical board (red LED should be on)