

Chapter 3

Output stages

3.1. Goals and properties

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- deliver power into the load with good efficacy and small power dissipate on the final transistors
- small output impedance
- maximum output excursion
- small distortions

Class A:

- very small distortions
- poor efficacy

Class B:

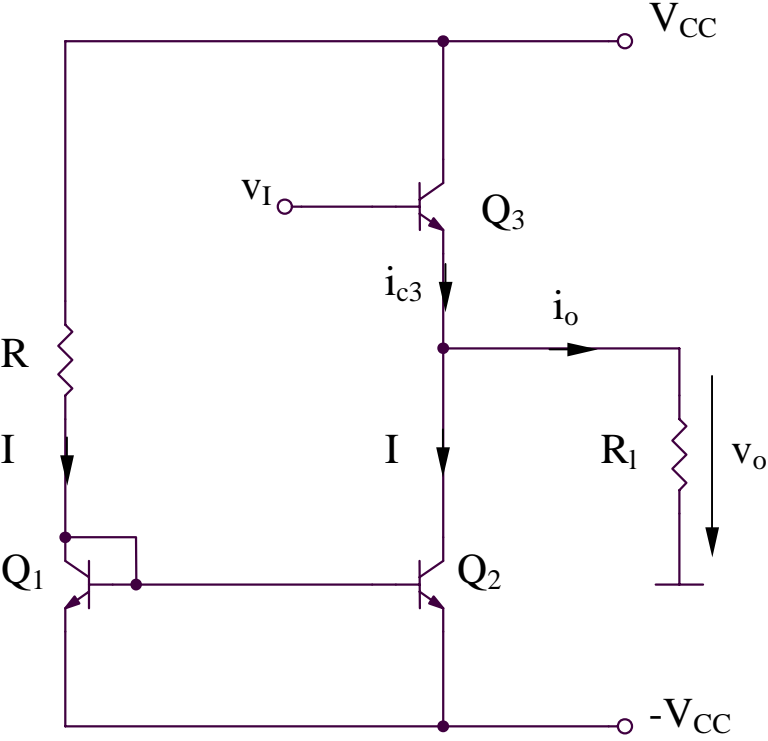
- important distortions
- good efficacy

Class AB:

- small distortions
- good efficacy

3.2. Class A output stage, common collector configuration

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In repose:

$$v_O = 0; i_O = 0$$

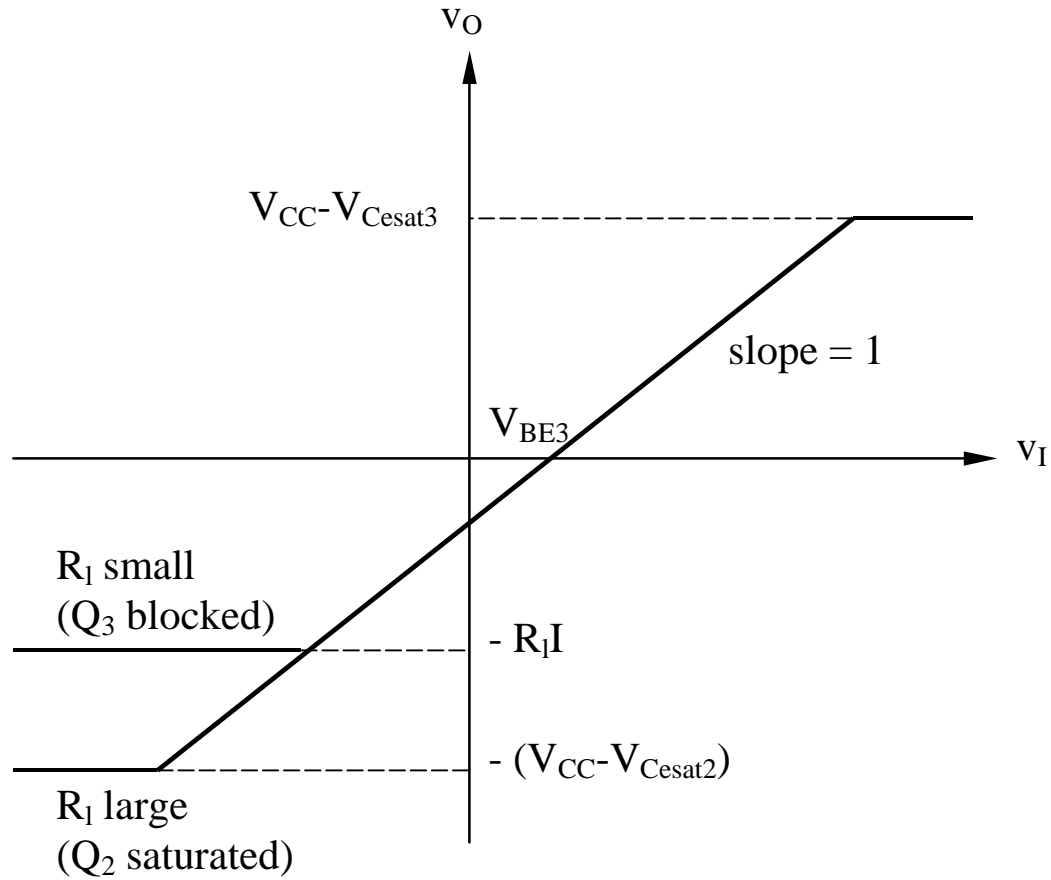
$$I_{C3} = I; V_{CE3} = V_{CC}$$

$$V_I = V_{BE3} = V_{th} \ln\left(\frac{I}{I_S}\right)$$

Transfer characteristic $v_O = f(v_I)$

$$\left. \begin{aligned} v_I &= v_{BE3} + v_O \\ v_{BE3} &= V_{th} \ln\left(\frac{i_{c3}}{I_S}\right) \\ i_{c3} &= I + \frac{v_O}{R_L} \end{aligned} \right\} \Rightarrow v_I = v_O + V_{th} \ln\left(\frac{I + \frac{v_O}{R_L}}{I_S}\right)$$

With $\frac{v_O}{R_L} \ll I$, $V_{th} \ln\left(\frac{I}{I_S}\right) = V_{BE3}$, the expression of the transfer characteristic becomes, in consequence, $v_I = v_O + v_{BE3}$ so linear.



$$i_{C3} = I + \frac{v_O}{R_1}$$

$$i_{C3} = I + \frac{V_{CC} - v_{CE3}}{R_1}$$

$$i_{C3} = 0 \Rightarrow v_{CE3} = V_{CC} + IR_1$$

The maximum positive value of the output voltage is:

$$V_{OM} = V_{CC} - V_{CEsat3}$$

The maximum negative output voltage depends on the value of R_1 :

- for large R_1 large, the negative limit of the output voltage is limited by the saturation of Q_2

$$V_{\overline{OM}} = V_{CC} - V_{CEsat2} \qquad I_{\overline{OM}} < I$$

- for R_1 small, the negative limit of the output voltage is limited by the blocking of Q_2

$$V_{\overline{OM}} = IR_1 < V_{CC} - V_{CEsat2} \qquad I_{\overline{OM}} = I$$

- It is possible to obtain in the same time maximum values of tension and current, so a maximum output power for an optimal value of the load resistance:

Fundamental energetical relations

Noting:

$$\hat{V}_O = KV_{CC}$$

where K is the utilization factor of the power supply, $0 \leq K < 1$. So:

$$\hat{I}_O = \frac{\hat{V}_O}{R_l} = \frac{KV_{CC}}{R_l} = KI$$

The power dissipated on Q_3 is:

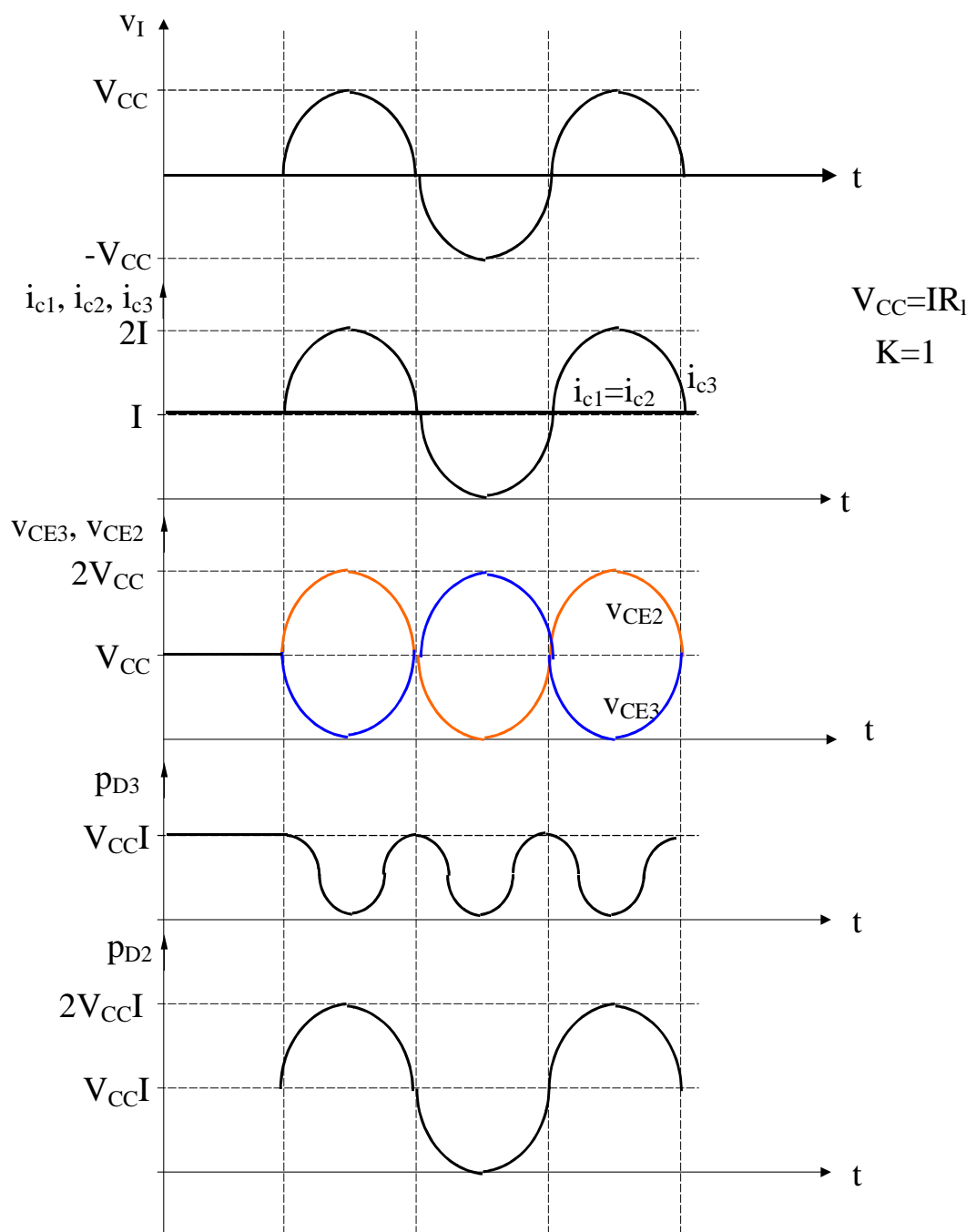
$$p_{D3} = v_{CE3}i_{C3} = \left(V_{CC} - \hat{V}_O \sin \omega t \right) \left(I + I_O \hat{\sin} \omega t \right)$$

$$p_{D3} = V_{CC}I(1 - K \sin \omega t)(1 + K \sin \omega t)$$

$$p_{D3} = V_{CC}I(1 - K^2 \sin^2 \omega t) = V_{CC}I \left(1 - \frac{K^2}{2} + \frac{K^2}{2} \cos 2\omega t \right)$$

So, the average power is:

$$P_{D3} = \frac{1}{2\pi} \int_0^{2\pi} p_{D3} d\omega t = V_{CC}I \left(1 - \frac{K^2}{2} \right)$$



The power dissipated on Q_2 is:

$$P_{D2} = i_{C2} v_{CE2} = I \left(V_{CC} + \hat{V}_O \sin \omega t \right) = IV_{CC} (1 + K \sin \omega t)$$

So, the average power is::

$$P_{D2} = \frac{1}{2\pi} \int_0^{2\pi} p_{D2} d\omega t = V_{CC} I$$

The consumed power could be written:

$$P_A = V_{CC} i_{C3} + V_{CC} i_{C2} = V_{CC} (2I + KI \sin \omega t)$$

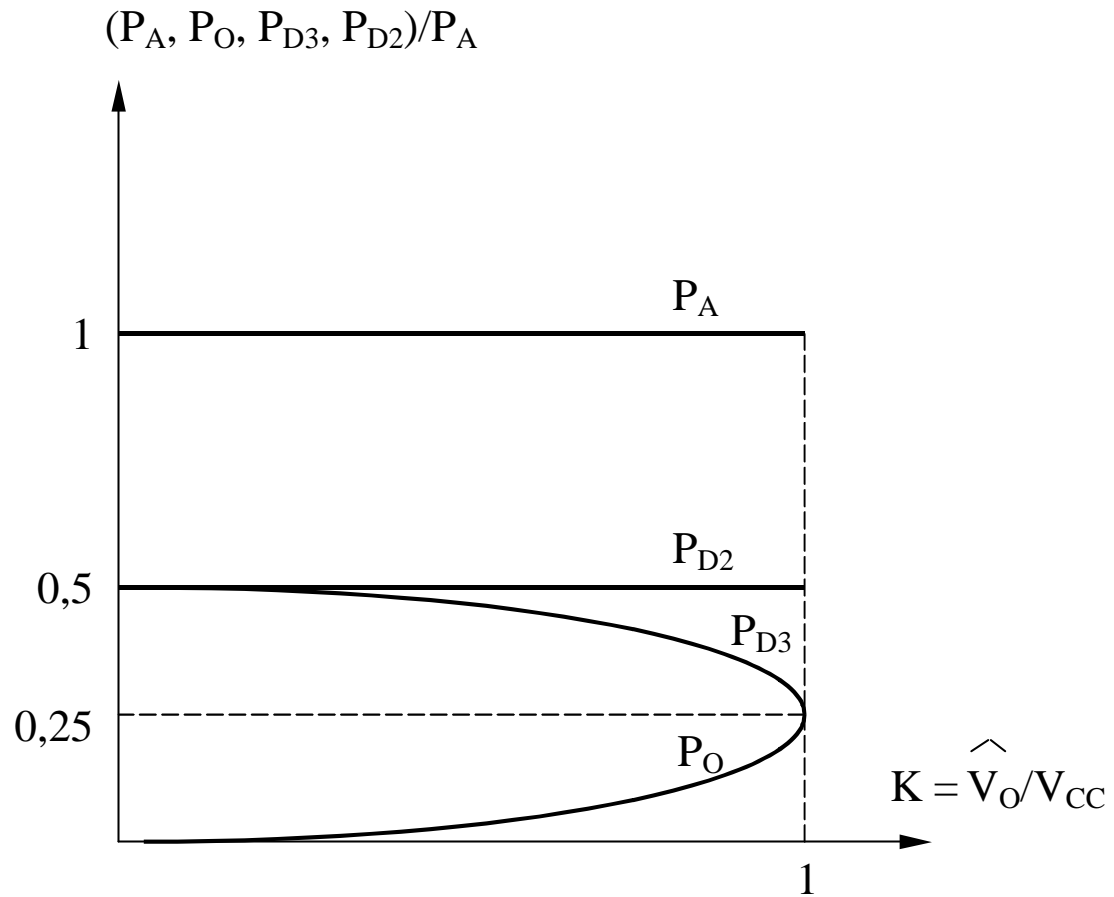
$$P_A = \frac{1}{2\pi} \int_0^{2\pi} p_A d\omega t = 2V_{CC} I$$

The average output power is:

$$P_O = \frac{1}{2\pi} \int_0^{2\pi} p_O d\omega t = \frac{1}{2\pi} \int_0^{2\pi} (KV_{CC} \sin \omega t)(KI \sin \omega t) d\omega t = \frac{K^2 V_{CC} I}{2}$$

$$\eta_A = \frac{P_O}{P_A} = 25\% K^2$$

so, a maximum value of 25%.

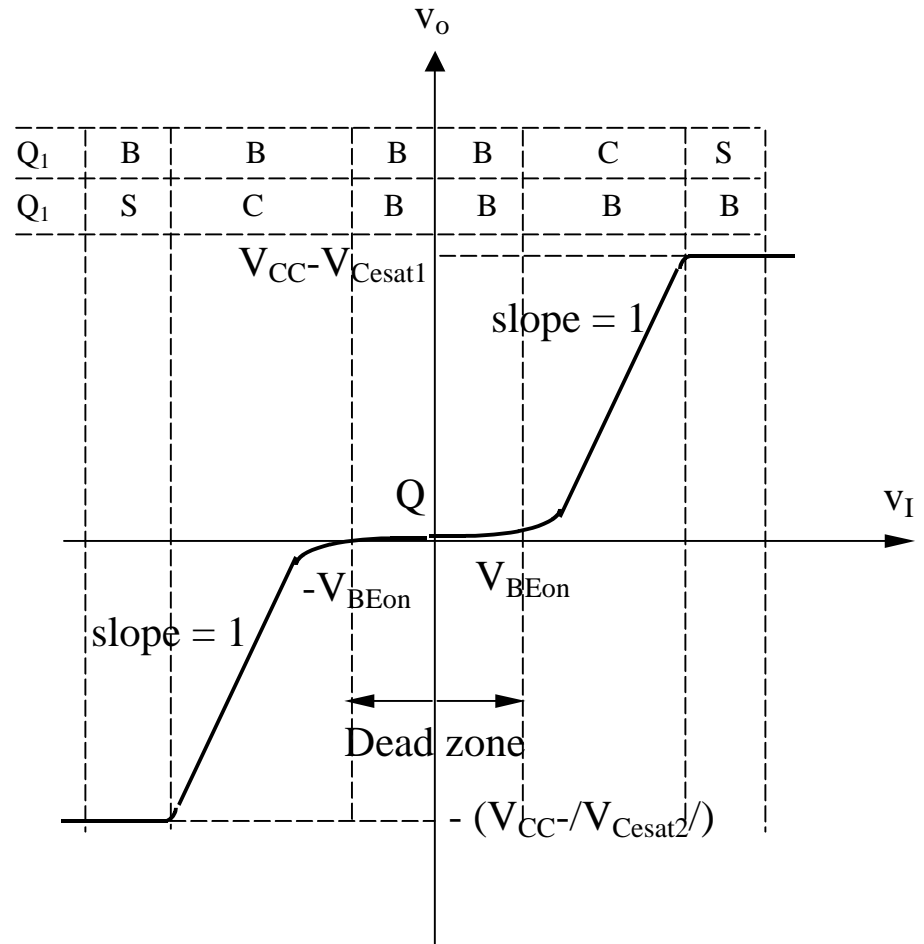
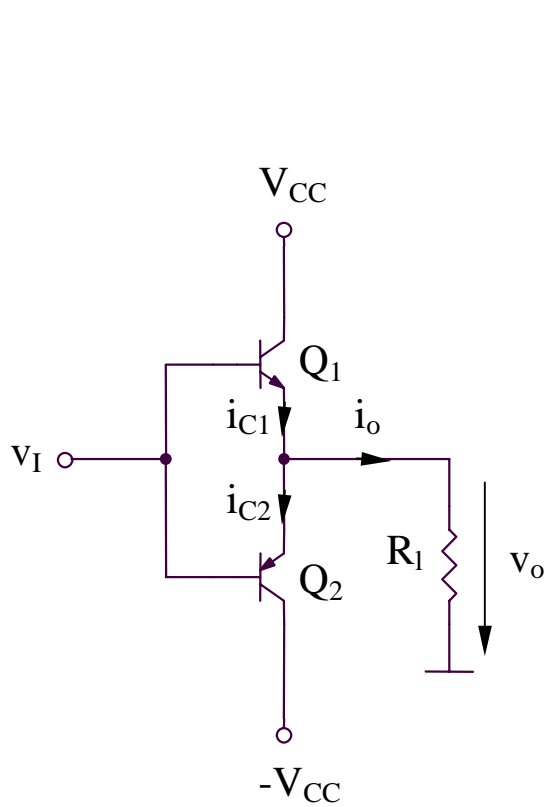


$$P_{D2} = P_{D3} + P_O$$

$$P_A = P_{D2} + P_{D3} + P_O = 2P_{D2}$$

3.3. Class B elementary output amplifier stage

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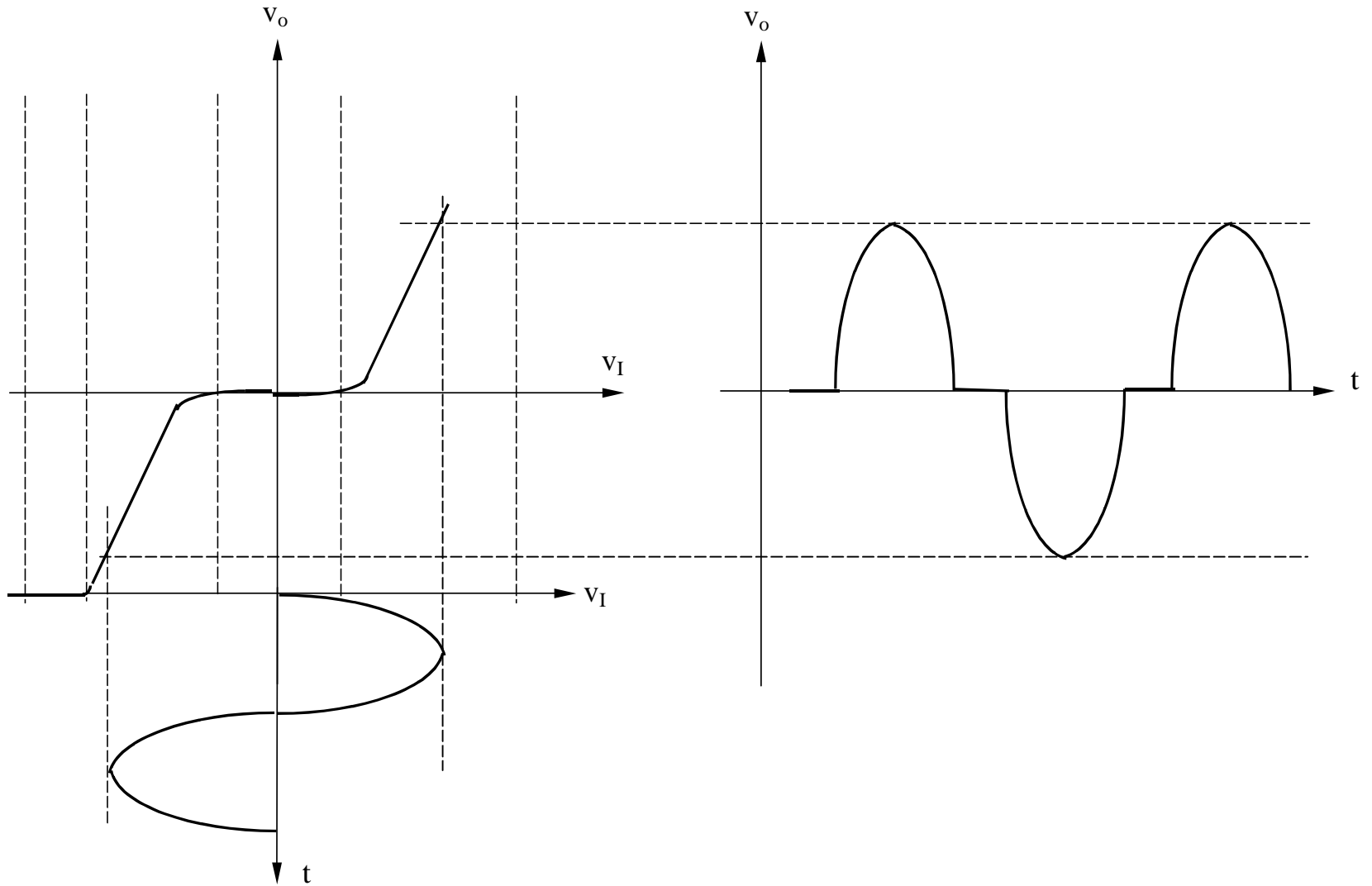


In repose:

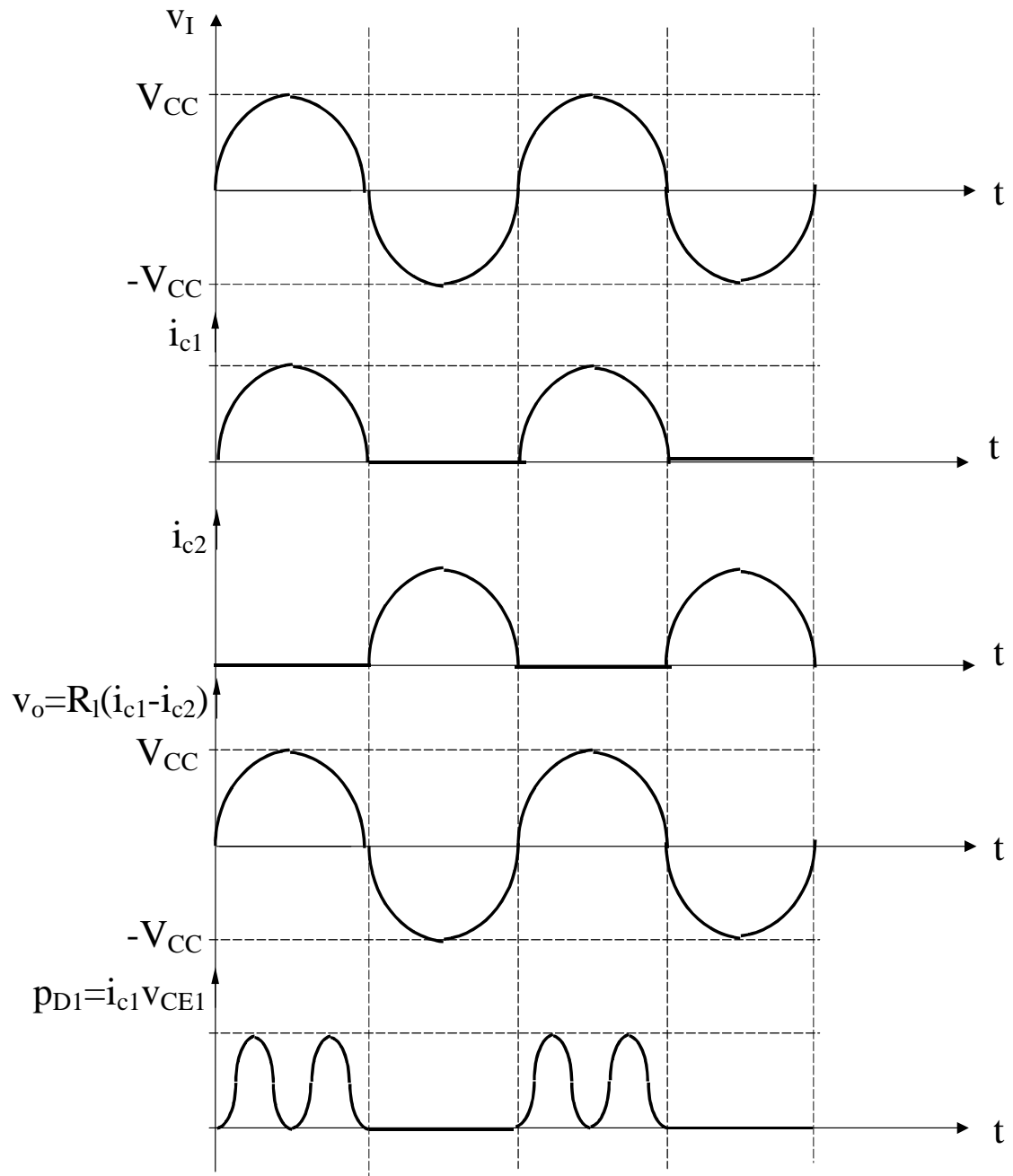
$$v_O = 0; i_O = 0; i_{c1} = i_{c2} = I; v_{BE1} + v_{EB2} = 0$$

If:

$$Q_1 \equiv Q_2; I_{S1} = I_{S2} = I_S \Rightarrow 2V_{th} \ln\left(\frac{I}{I_S} + 1\right) = 0 \Rightarrow I = 0 \Rightarrow i_{c1} = i_{c2} = 0$$



Transfer characteristic



Disadvantages of a push-pull class B output stage

- “dead” zone (distortions)
- requires PNP transistors (non-performant)

Solutions:

- evolution to class AB
- solution “full NPN”

Fundamental energetical relations

Noting:

$$\hat{V}_O = KV_{CC}$$

where K is the utilization factor of the supply voltage, $0 \leq K < 1$.

The average output power P_O is:

$$P_O = \frac{1}{2\pi} \int_0^{2\pi} p_O d\omega t = \frac{1}{2\pi} \int_0^{2\pi} (KV_{CC} \sin \omega t) \left(K \frac{V_{CC}}{R_l} \sin \omega t \right) d\omega t = \frac{K^2 V_{CC}^2}{2R_l}$$

Noting with P_A the total delivered power (for both supply sources):

$$P_A = 2V_{CC}I_{CC}$$

Where the continuous component I_{CC} is:

$$I_{CC} = \frac{1}{2\pi} \int_0^{\pi} I_C \sin \omega t d\omega t = \frac{1}{\pi} \hat{I}_C = \frac{1}{\pi} \frac{\hat{V}_O}{R_l} = \frac{KV_{CC}}{\pi R_l}$$

So::

$$P_A = K \frac{2V_{CC}^2}{\pi R_l}$$

The average dissipated power P_D for a pair of transistors in class B is:

$$P_D = P_A - P_O = \frac{V_{CC}^2}{2R_l} \left(\frac{4K}{\pi} - K^2 \right)$$

The previous expression represents a parabola in K, so the maximum could be obtained by making the derivate equal with zero:

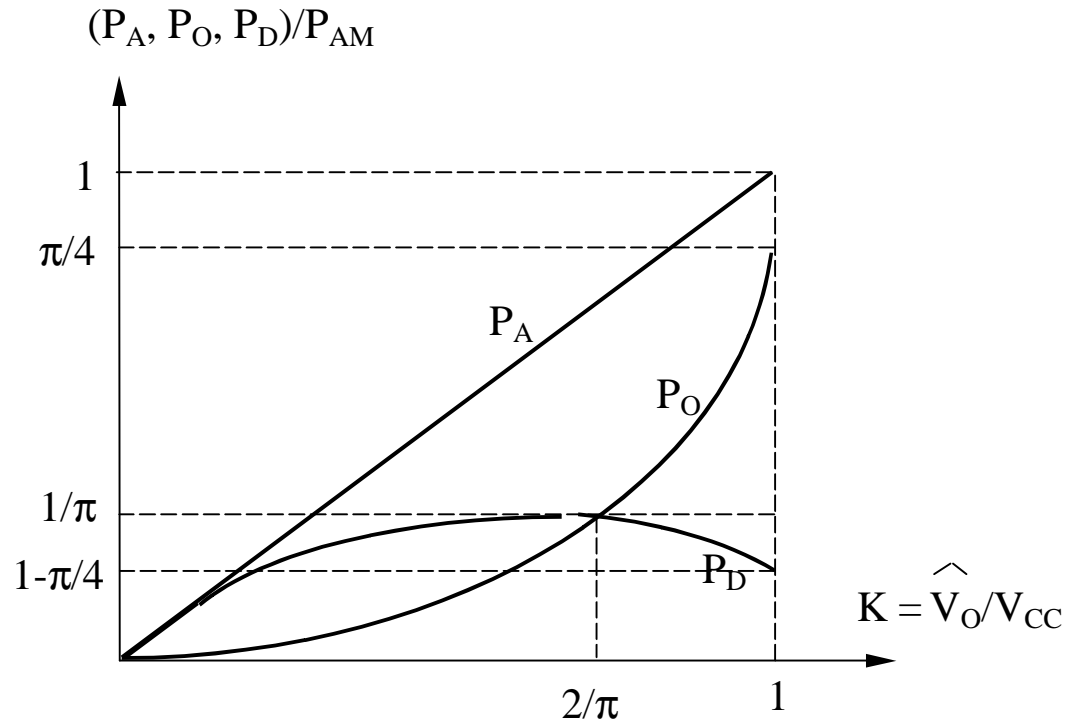
$$\frac{4}{\pi} - 2K = 0 \Rightarrow K = \frac{2}{\pi}$$

For this value of K it will be obtained the maximum average dissipated power (for both transistors):

$$P_{DM} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R_l} = \frac{4}{\pi^2} \frac{V_{CC}^2}{2R_l} = \frac{4}{\pi^2} P_{OM} \qquad P_{OM} = \frac{V_{CC}^2}{2R_l}$$

On the following graphics it will be represented the normalized powers as function of K.

$$\frac{P_A}{P_{AM}} = K; \quad \frac{P_O}{P_{AM}} = \frac{\pi K^2}{4}; \quad \frac{P_D}{P_{AM}} = K \left(1 - \frac{K\pi}{4} \right)$$



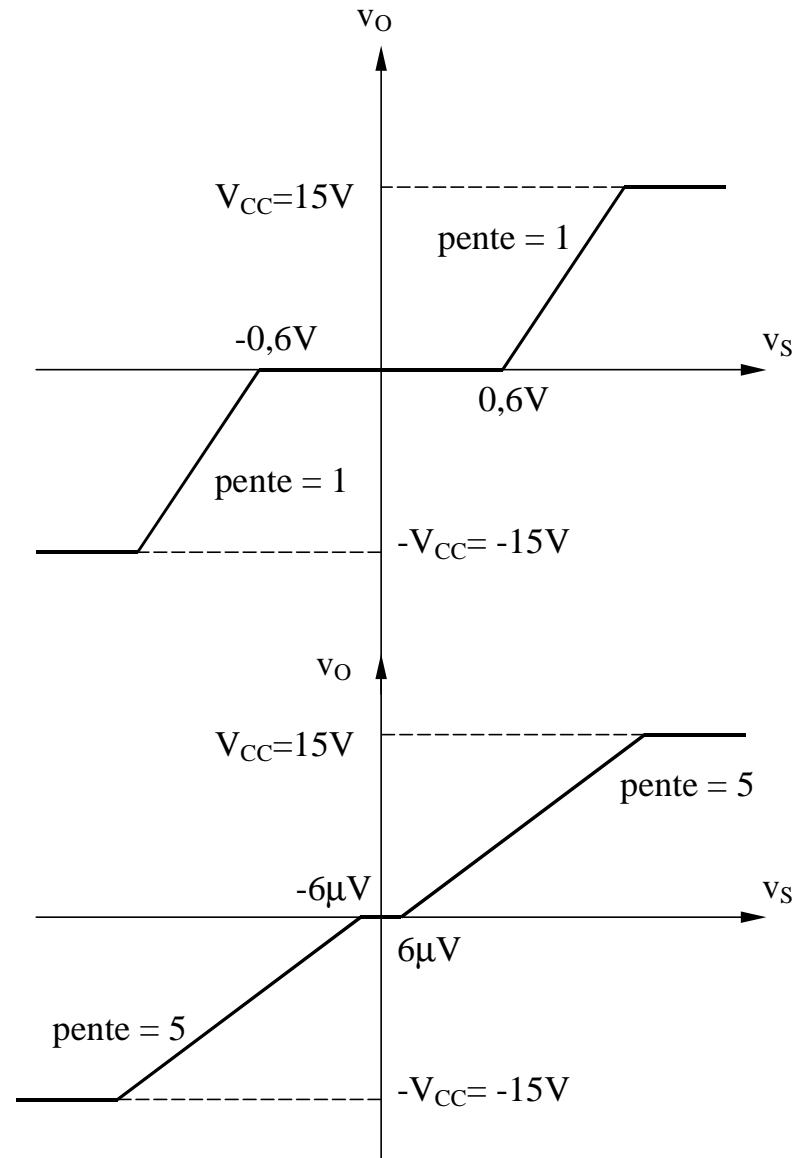
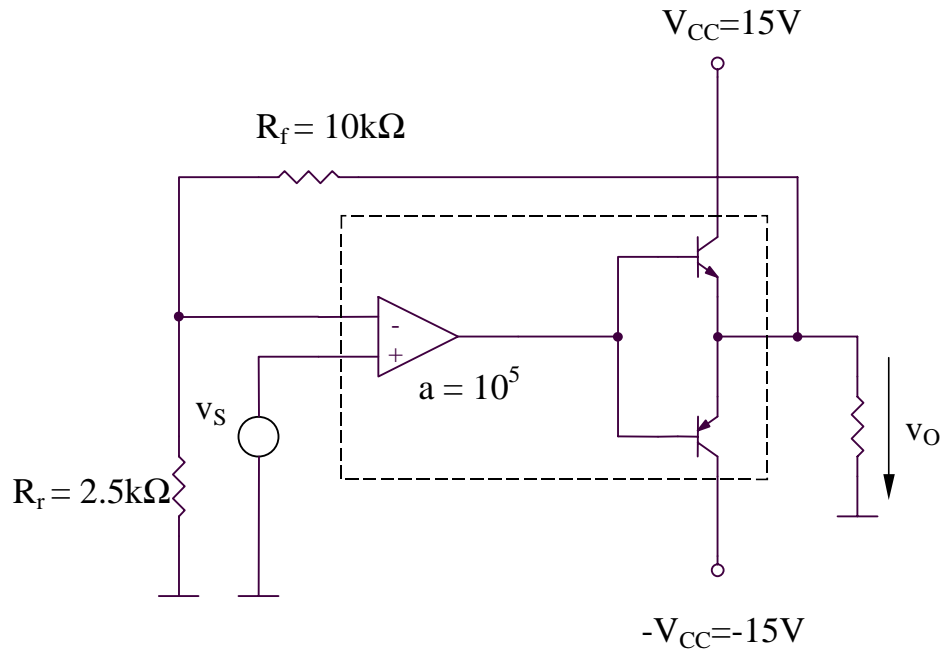
The efficacy depends on the amplitude of the output power:

$$\eta = \frac{P_O}{P_A} = K \frac{\pi}{4}$$

Its maximum is obtained for $K=1$ and it is $\pi/4$ (78.5%).

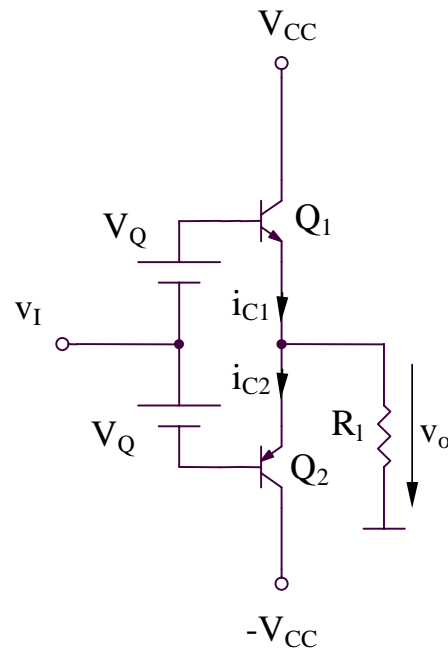
3.4. The nonlinearity reduction for a class B output stage due to the negative reaction

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3.5. Class AB output stage

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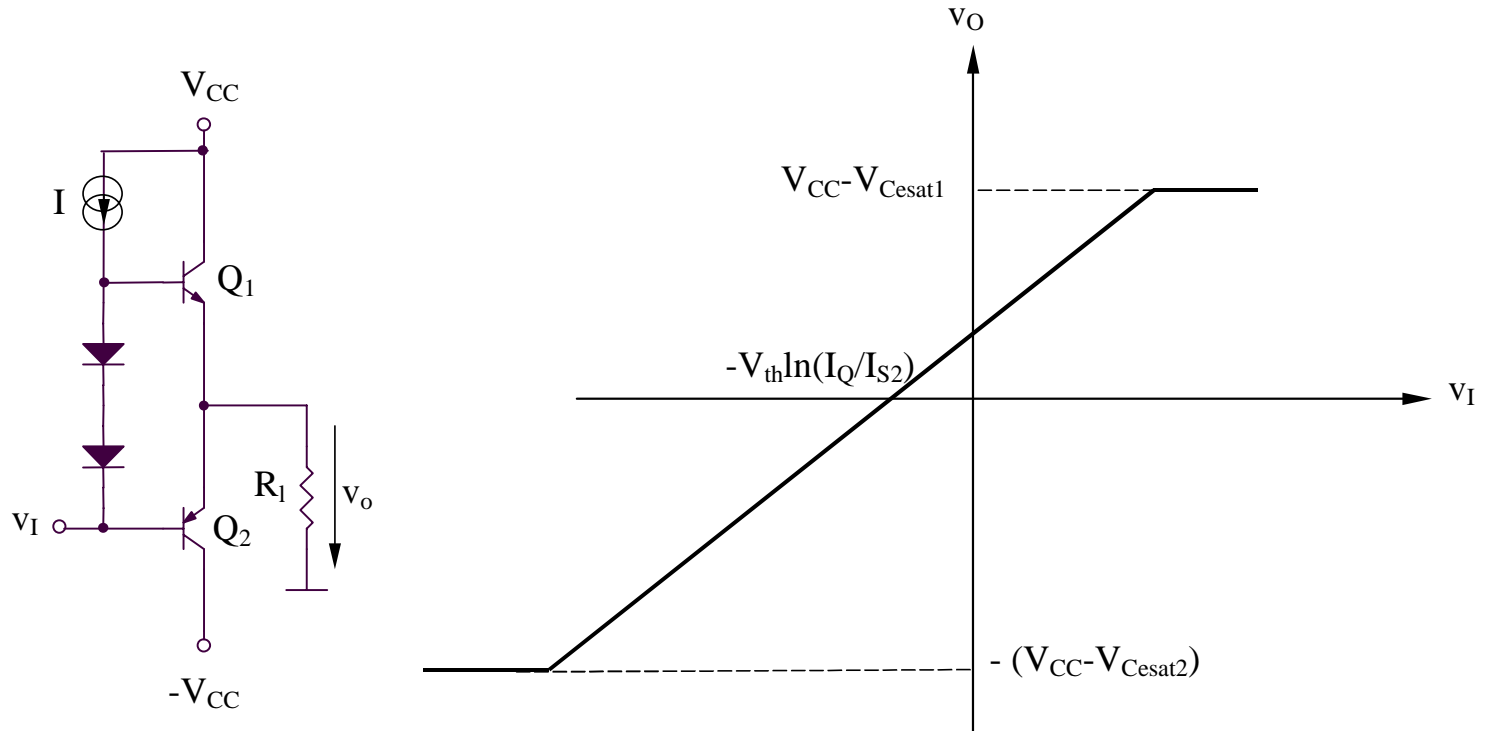


In order to obtain a good linearity of the global transfer characteristic, it is necessary to:

- have a good matching between the transistors from the circuit
- proper choose of biasing voltage in repose
- choose a pre-biasing of the output stage in order to avoid the thermal embalmment

Circuit for avoiding the thermal embalmment (1)

The biasing voltage of the output stage must be a temperature-dependent voltage (for example, the base-emitter voltage)

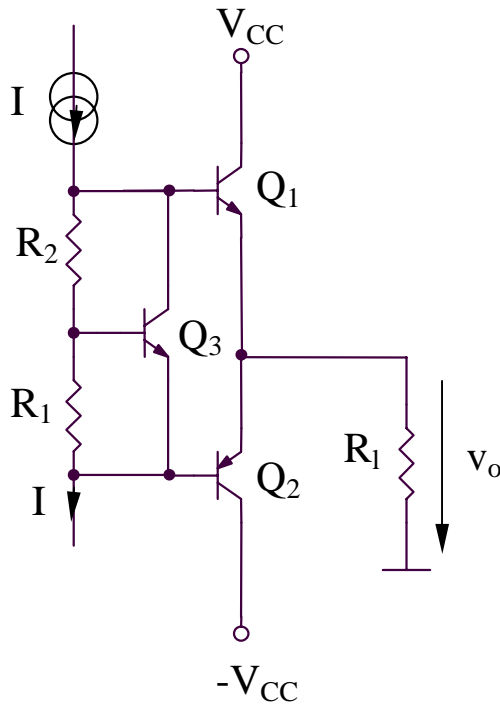


The diode-connected transistors must be at the same temperature with the final transistors. In repose :

$$v_o = 0 \Rightarrow I_{QC1} = I_{QC2} = I_Q$$

$$V_{BE1} + V_{EB2} = 2V_D \Rightarrow V_{th} \ln\left(\frac{I_Q}{I_{S1}} \frac{I_Q}{I_{S2}}\right) = 2V_{th} \ln\left(\frac{I}{I_{SD}}\right) \Rightarrow I_Q = I \frac{\sqrt{I_{S1} I_{S2}}}{I_{SD}}$$

Circuit for avoiding the thermal embalmment (2)

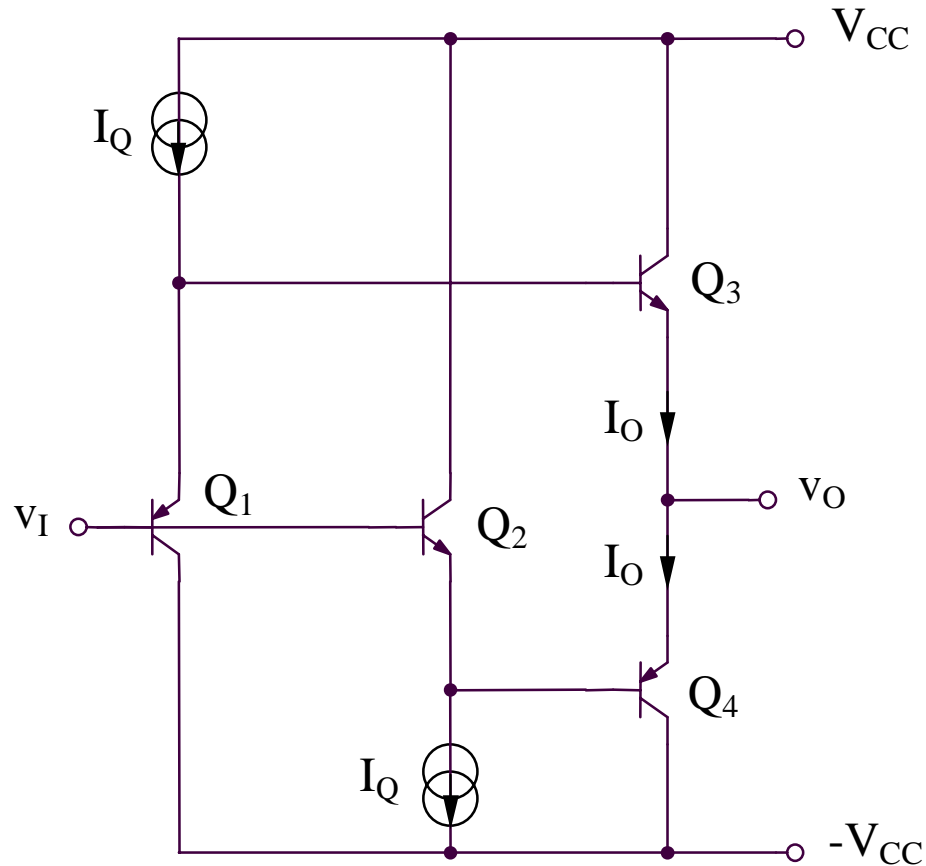


$$\left. \begin{aligned} v_{BE1} + v_{EB2} &= v_{CE3} \\ v_{CE3} &= \frac{v_{BE3}}{R_1} (R_1 + R_2) \end{aligned} \right\} \Rightarrow$$

$$\Rightarrow V_{th} \left(\ln \frac{I_Q}{I_{S1}} + \ln \frac{I_Q}{I_{S2}} \right) = \left(1 + \frac{R_2}{R_1} \right) V_{th} \ln \frac{I}{I_{S3}}$$

$$\Rightarrow I_Q = \sqrt{I_{S1} I_{S2} \left(\frac{I}{I_{S3}} \right)^{1 + \frac{R_2}{R_1}}}$$

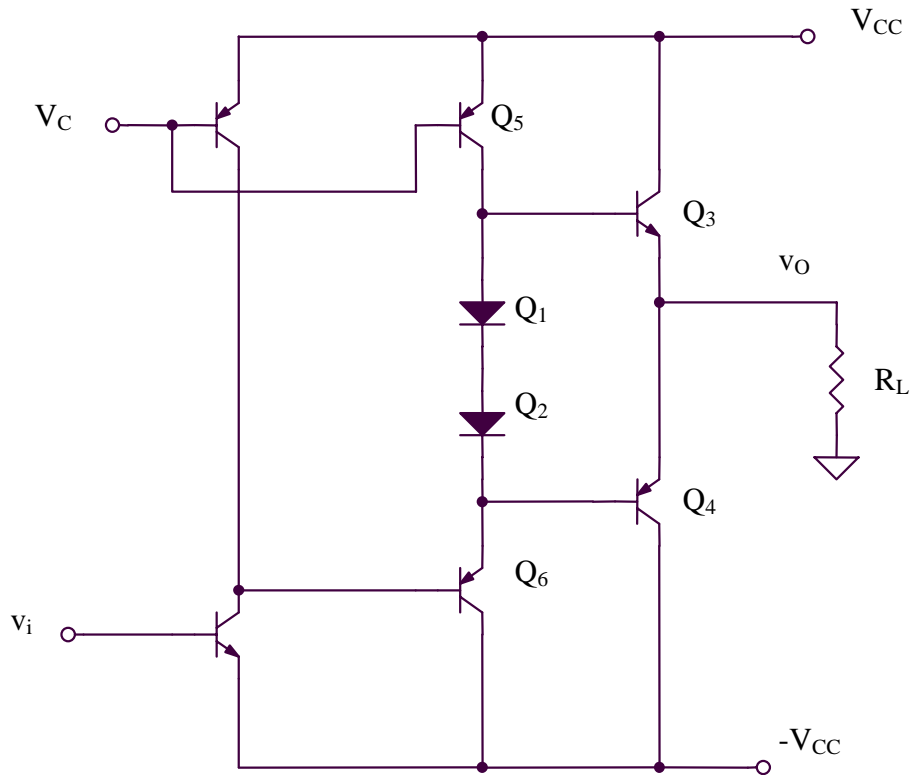
Circuit for avoiding the thermal embalmment (3)



$$|V_{BE1}| + V_{BE2} = V_{BE3} + |V_{BE4}|$$

$$2V_{th} \ln \frac{I_Q}{I_S} = 2V_{th} \ln \frac{I_O}{I_S} \Rightarrow I_O = I_Q$$

Circuit for avoiding the thermal embalmment (4)



$$V_{BE1} + V_{BE2} = V_{BE3} + V_{BE4}$$

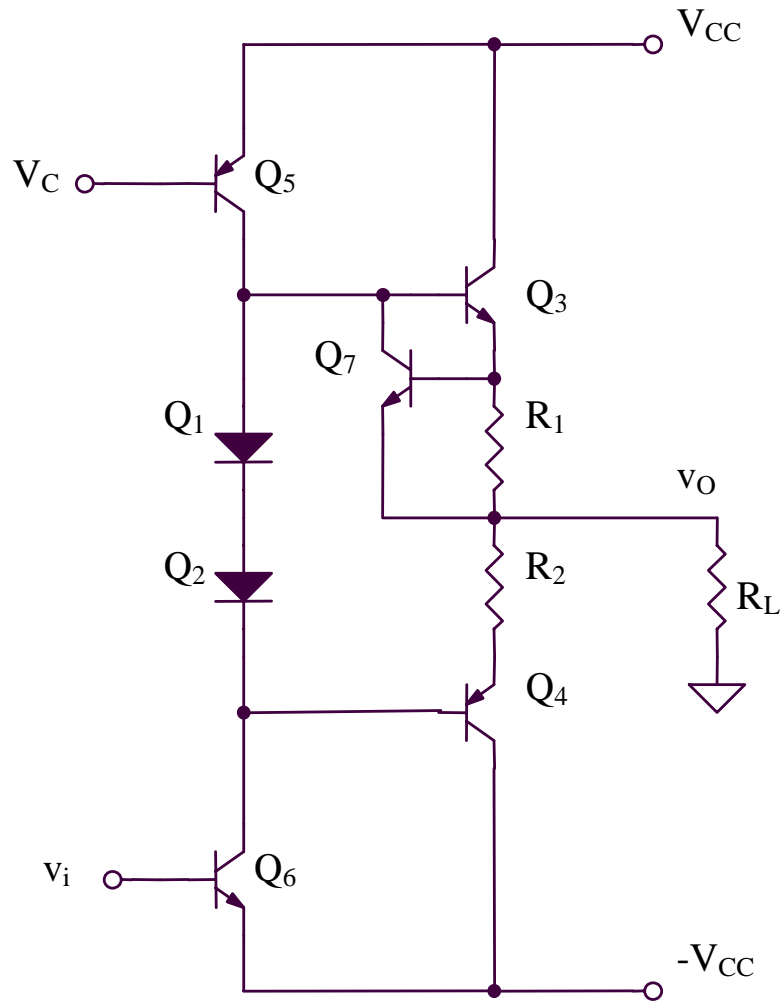
$$V_{th} \ln \frac{I_{C1}}{I_{S1}} + V_{th} \ln \frac{I_{C2}}{I_{S2}} = V_{th} \ln \frac{I_{C3}}{I_{S3}} + V_{th} \ln \frac{I_{C4}}{I_{S4}}$$

$$\Rightarrow I_{C3} = I_{C4} = I_{C1} \sqrt{\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}}$$

$$V_{Omax}^+ = V_{CC} - V_{EC5sat} - V_{BE3}$$

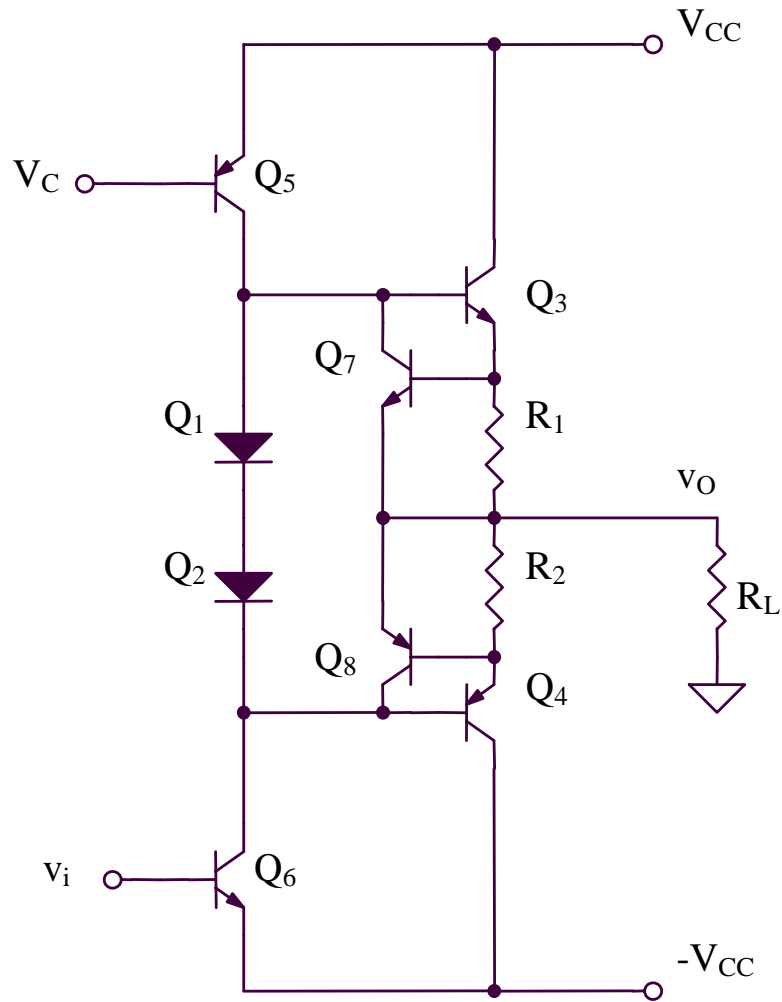
$$V_{Omax}^- = -V_{CC} + V_{EC6sat} - V_{BE4}$$

Circuit with overload protection (1)



$$I_{Omax}^+ = \frac{V_{BE7}}{R_1}$$

Circuit with overload protection (2)



$$I_{Omax}^+ = \frac{V_{BE7}}{R_1}$$

$$I_{Omax}^- = \frac{V_{EB8}}{R_2}$$