

# Wien Bridge Oscillator

It is required to design a Wien Bridge Oscillator with the following specifications:

- ◆ Oscillation frequency : programmable in  $N \div 2N$  [KHz] range;
  - ◆ Output load impedance  $(N/5)$  [ $k\Omega$ ];
  - ◆ The gain of the internal amplifier is automatically adjusted by using a FET;
  - ◆ The output amplitude may be adjusted in  $(0 \div ((N/5) \cdot V_{p-p}))$  range .
- ,where N is the index from the catalog of each student.

The circuit will be practically implemented on a PCB. There are two options:

- a. **SMT & PCB technology (maximum points = 100)**
- b. **THD/SMD (perfo-board) technology (maximum points = 80)**

a. **For SMT & PCB technology, the following requirements should be met:**

- ◆ PCB dimensions: 40mm x 40mm;
- ◆ Board is double sided, FR4, copper width 35  $\mu$ m, board width 1,6mm;
- ◆ All components are placed on the TOP side;
- ◆ It will be used only SMD passive components from 0805 series;
- ◆ It will be used only SMD FET, MOSFET and bipolar transistors (SOT-23, D-PAK cases)
- ◆ Circular test points (maximum 5) – justified by the test plan
- ◆ The interconnection structure may contain 0 $\Omega$  resistors SMD1206, the maximum number of 0 ohms resistors is 5;
- ◆ The origin (0,0) is placed in the bottom left corner of the PCB, all coordinates have positive values;
- ◆ A clearance of 50 mil will be kept from the margins of the board;
- ◆ The silkscreen should not appear on the pads of the components;
- ◆ A mechanical layer will be generated. This will contain the board outline, the drill drawing, the drill chart/table, drill legend, the layer stack-up and mechanical information for PCB manufacturing.
- ◆ The dimension quotes of the PCB shouldn't appear on the TOP side. If these quotes exist, they should appear on a non-electrical mechanical layer;
- ◆ The board will be provided with identification information about the designer (Last Name, First Name, Group, PDCE I 2016-2017).

The Gerber files-274x standard should contain the following informations:

- ◆ board outline;
- ◆ electrical layer TOP;
- ◆ electrical layer BOTTOM;
- ◆ non-electrical layer Silk Screen Top;
- ◆ non-electrical layer Solder Mask Top;
- ◆ non-electrical layer Solder Paste Top;
- ◆ the aperture list and the drilling file

The following widths are recommendend for the routing layers:

- ◆ 1A current – 40 mils;
- ◆ Few hundreds mA currents - 32 mils;
- ◆ Signal - 20 mils
- ◆ Spacing 12 mils.
- ◆ The via hole diameter is 0.4mm

The OrCAD program – Lite version (available for download <http://www.cetti.ro/v2/orcad16.php> ) with imposed limitations will be used for circuit simulation and layout design.

***The components which may be used for the project are listed in Annex 1.***

Deadlines:

1. Examination - max. 60 pct.

Until the end of the V<sup>th</sup> week will be accomplished:

- ◆ Analytical calculation and the simmlations of the chosen circuit diagram.

Until the end of the VII<sup>th</sup> week will be accomplished:

- ◆ The Gerber files for the layout ( 274x standard)
- ◆ Bill of Materials (BOM) file.

If the above requests are fully met with no deadline extension, a mark of maximum 60 points will be granted. If the requests are not fully met, the student will not qualify for practical design – in this situation the final mark for Project 1 will be lower than 6.

2. Final examination - max. 40 pts.

It will be accomplished in the last 2 weeks of the semester. The project in final form will be delivered (paper form and electronic form, on a CD – containing the document, calculations and simulations). The practical design remains in the faculty property.

**b. For THD/SMD (perfo-board) technology (maximum points = 80), the following requirements should be accomplished:**

Deadlines:

1. Examination - max. 60 pct.

Until the end of the VII<sup>th</sup> week will be accomplished:

- ◆ Analytical calculation and the simulations of the chosen circuit diagram.

Until the end of the VIII<sup>th</sup> week will be accomplished:

- ◆ Bill of Materials (BOM) file.

If the above requests are fully met with no deadline extension, a mark of maximum 60 points will be granted. If the requests are not fully met, the student will not qualify for practical design – in this situation the final mark for Project 1 will be lower than 6.

2. Final examination - max. 20 pts.

It will be accomplished in the last 2 weeks of the semester. The project in final form will be delivered (paper form and electronic form, on a CD – containing the document, calculations and simulations). The practical design remains in the faculty property.

**The minimal content of the project (if one of the requirements 1-3 are not fulfilled, the student will not pass the exam!):**

**1. The block diagram of the circuit**

**2. The detailed schematic diagram and the calculations for each functional block and each component.**

- *The passive components will have standard values*
- *The semiconductor parameters will not exceed the values from the datasheets*
- *The choice of a certain component will be justified by calculation*
- *It will be demonstrate a reliable operation for each component. (for example, for a bipolar transistor it will be justified that the maximum absolute values from the datasheet are not reached -  $I_{CMAX}$ ,  $V_{CEMAX}$ ,  $P_{dMAX}$ )*
- *The calculus should demonstrate that the imposed specifications of the design are fulfilled.*

**3. PSPICE simulations (.CIR files, the waveforms, bias points, etc.)**

4. PCB Layout (including all layers).

5. The TOP image of the designed PCB.

6. The BOTTOM image of the designed PCB.

7. The Silk screen TOP layer;

8. The Solder Mask TOP layer;

9. The Solder Paste TOP layer.

10. The mechanical layer.

11. Experimental results and measurements.

12. A chapter which includes a short form of a user manual for the designed circuit for potential customers.

13. Power Point presentation of the Project (10 minutea)

**Bibliography:**

1. P. R. Gray, P. J Hurst, S. H. Lewis, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, J. Wiley & Sons, 2001.

2. A. M. Manolescu, A. Manolescu, *Analog Integrated Circuits*, Ed. Electronica 2000, București, 2011.
3. D. Self, *Audio Power Amplifier Design Handbook*, Fourth edition, Newnes, 2006.
4. G. A. Rincon-Mora, *Voltage References – from Diodes to Precision High-Order Bandgap Circuits*, John Wiley, 2001.
5. L. Teodorescu, [http://wiki.dcae.pub.ro/images/3/34/Signal\\_generator.pdf](http://wiki.dcae.pub.ro/images/3/34/Signal_generator.pdf)[http://wiki.dcae.pub.ro/index.php/Project\\_1\\_-\\_Electronic\\_Devices\\_and\\_Circuits](http://wiki.dcae.pub.ro/index.php/Project_1_-_Electronic_Devices_and_Circuits)
6. L. Teodorescu, [http://wiki.dcae.pub.ro/images/7/79/Linear\\_regulator.pdf](http://wiki.dcae.pub.ro/images/7/79/Linear_regulator.pdf)
7. L. Teodorescu, Project 1 - Electronic Devices and Circuits, [http://wiki.dcae.pub.ro/index.php/Project\\_1\\_-\\_Electronic\\_Devices\\_and\\_Circuits](http://wiki.dcae.pub.ro/index.php/Project_1_-_Electronic_Devices_and_Circuits)
8. T.L. Floyd, *Electronic Devices- Electron Flow Version*, 9<sup>th</sup> edition, Prentice Hall, 2012;
9. C.G. Fonstad, *Microelectronic Devices and Circuits*, McGraw-Hill, 1994
10. B. Razavi, *Fundamentals of Microelectronics*, 2<sup>nd</sup> edition, Wiley Global Education, 2013