Chapter 4

Output stages

4.1. Goals and properties

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• deliver power into the load with good efficacy and small power dissipate on the final transistors
• small output impedance
• maximum output excursion
• small distortions

Class A:

- very small distortions
- poor efficacy

Class B:

- important distortions
- good efficacy

Class AB:

- small distortions
- good efficacy

4.2. Class A output stage, common collector configuration

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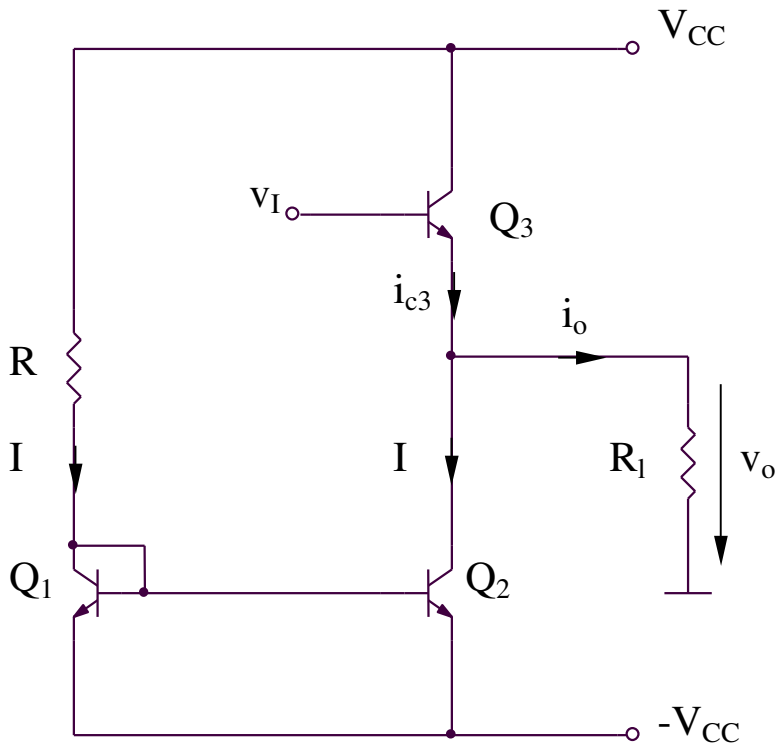


In repose:

$$v_O = 0; i_O = 0$$

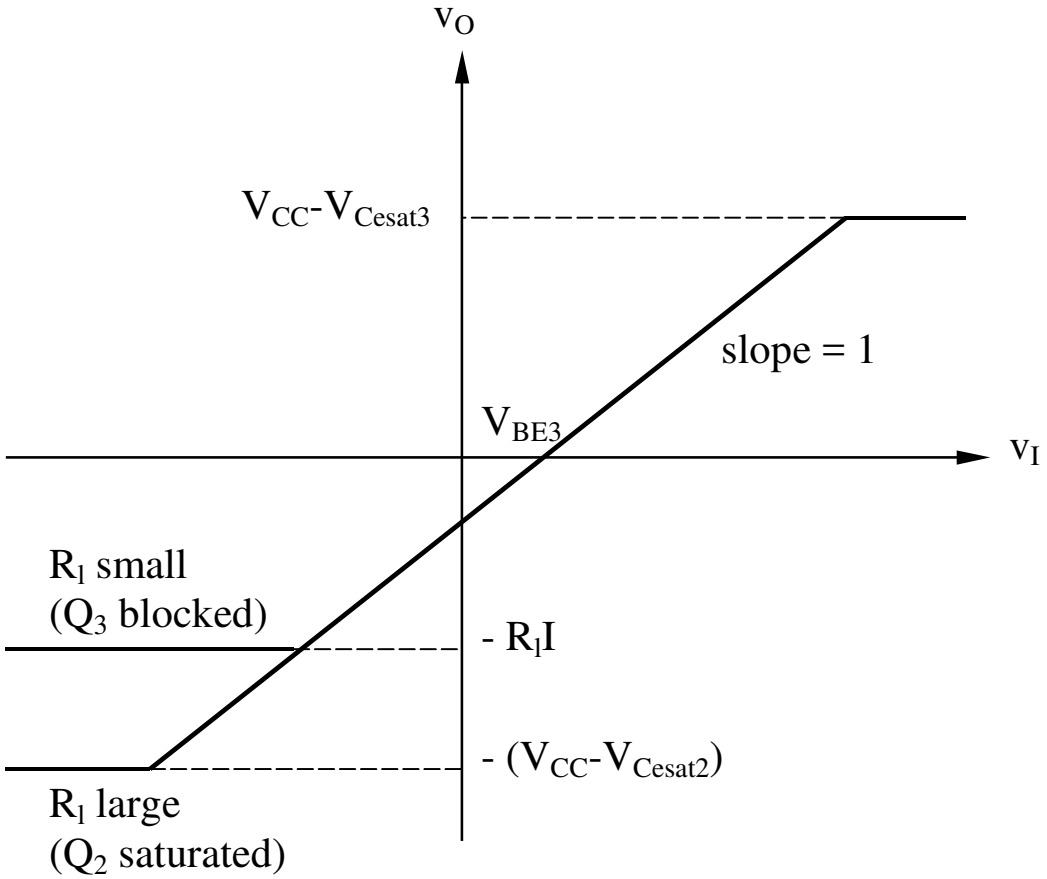
$$I_{C3} = I; V_{CE3} = V_{CC}$$

$$V_I = V_{BE3} = V_{th} \ln\left(\frac{I}{I_S}\right)$$

Transfer characteristic $v_O = f(v_I)$

$$\left.\begin{array}{l} v_I = v_{BE3} + v_O \\ v_{BE3} = V_{th} \ln\left(\dfrac{i_{c3}}{I_S}\right) \\ i_{c3} = I + \dfrac{v_O}{R_l} \end{array}\right\} \Rightarrow v_I = v_O + V_{th} \ln\left(\frac{I + \dfrac{v_O}{R_l}}{I_S}\right)$$

With $\dfrac{v_O}{R_l} << I$, $V_{th} \ln\left(\dfrac{I}{I_S}\right) = V_{BE3}$, the expression of the transfer characteristic becomes, in consequence, $v_I = v_O + v_{BE3}$ so linear.



$$i_{C3} = I + \frac{v_O}{R_l}$$

$$i_{C3} = 0 \Rightarrow v_{CE3} = V_{CC} + IR_l$$

$$i_{C3} = I + \frac{V_{CC} - v_{CE3}}{R_l}$$

The maximum positive value of the output voltage is:

$$V_{OM} = V_{CC} - V_{CEsat3}$$

The maximum negative output voltage depends on the value of R_l :

- for large R_l large, the negative limit of the output voltage is limited by the saturation of Q_2

$$V_{OM}^{-} = V_{CC} - V_{CEsat2} \qquad I_{OM}^{-} < I$$

- for R_l small, the negative limit of the output voltage is limited by the blocking of Q_2

$$V_{OM}^{-} = IR_l < V_{CC} - V_{CEsat2} \qquad I_{OM}^{-} = I$$

•It is possible to obtain in the same time maximum values of tension and current, so a maximum output power for an optimal value of the load resistance:

4.3. Class B elementary output amplifier stage

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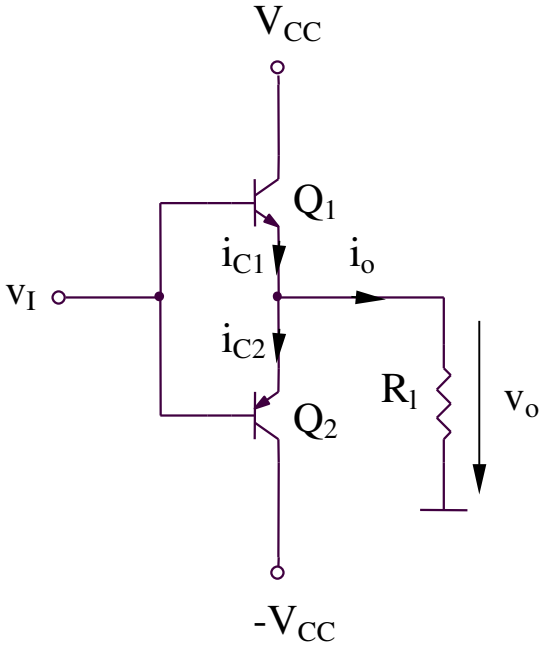
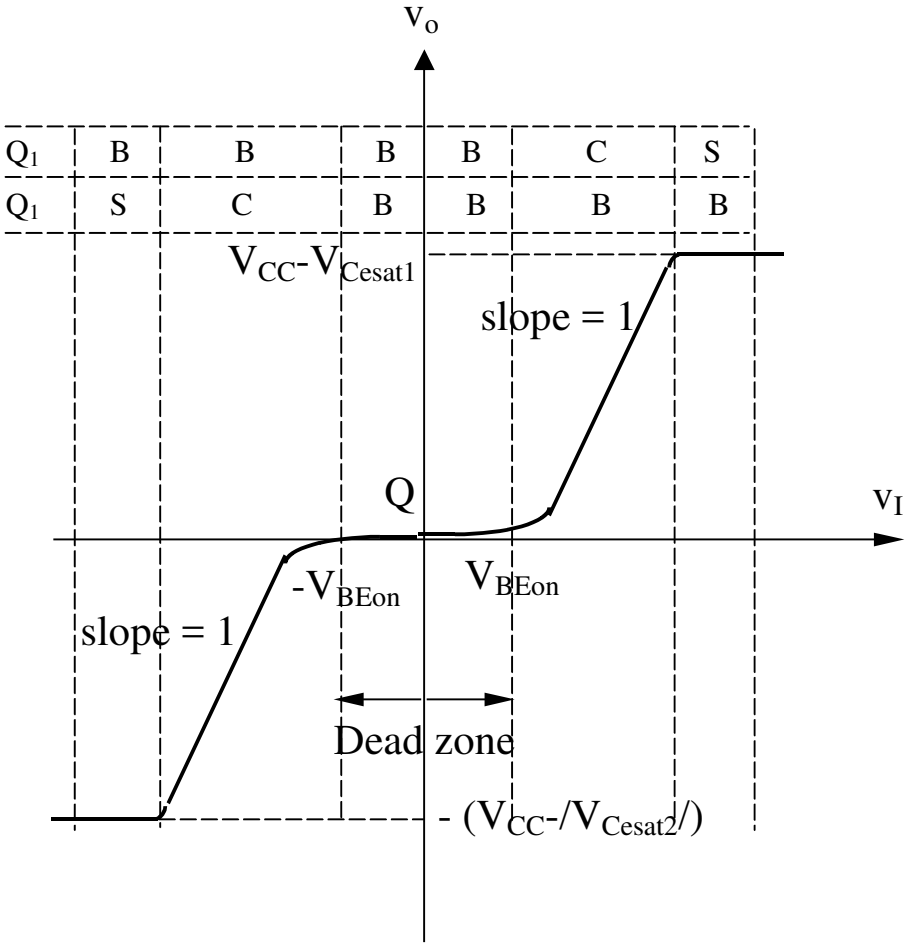


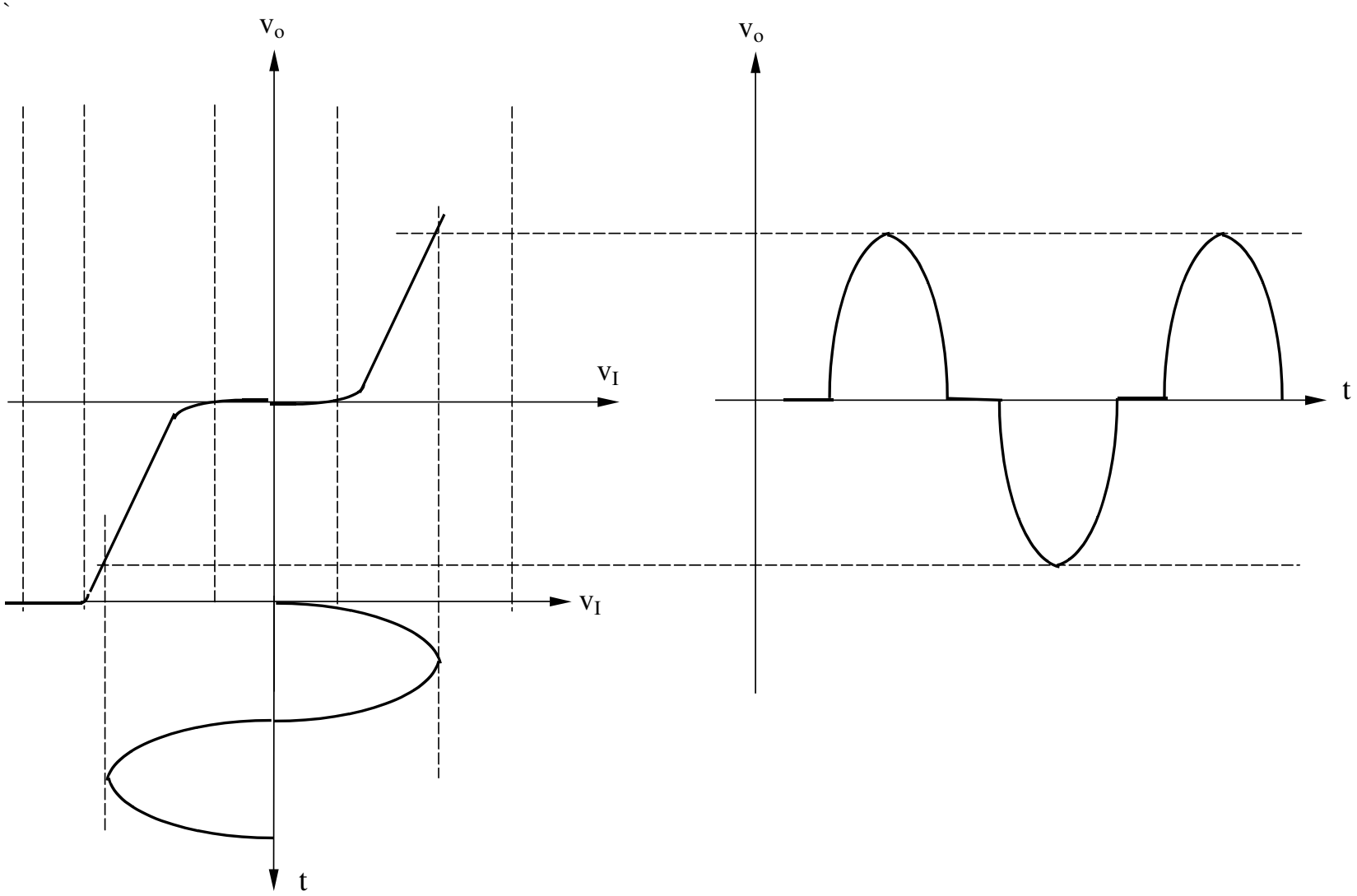


In repose:

$$v_O = 0;\ i_O = 0;\ i_{c1} = i_{c2} = I;\ v_{BE1} + v_{EB2} = 0$$

If:

$$Q_1 \equiv Q_2;\ I_{S1} = I_{S2} = I_S \Rightarrow 2V_{th} \ln\left(\frac{I}{I_S} + 1\right) = 0 \Rightarrow I = 0 \Rightarrow i_{c1} = i_{c2} = 0$$



Transfer characteristic

4.4. The nonlinearity reduction for a class B output stage due to the negative reaction

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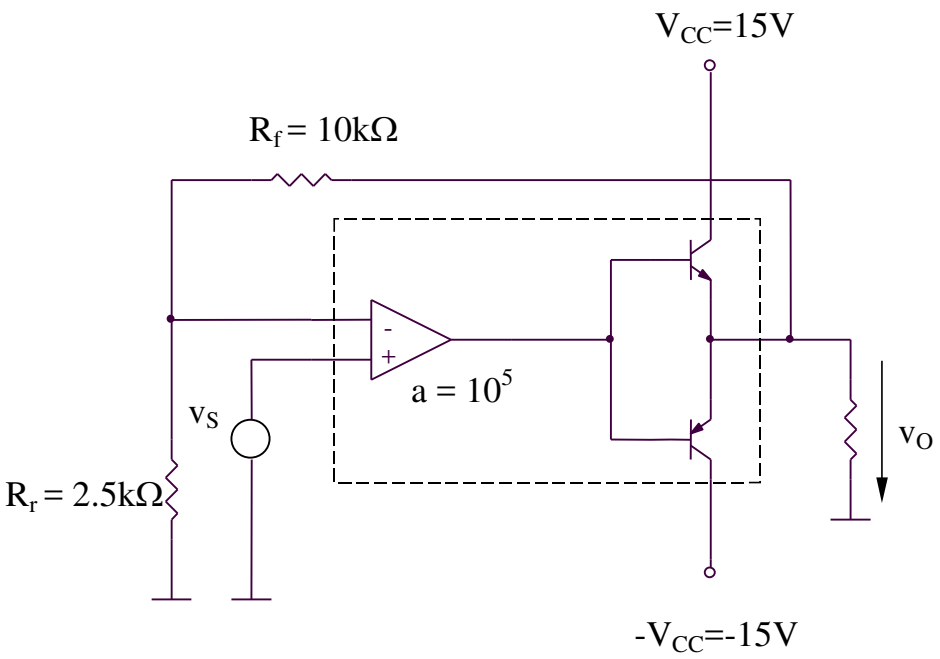

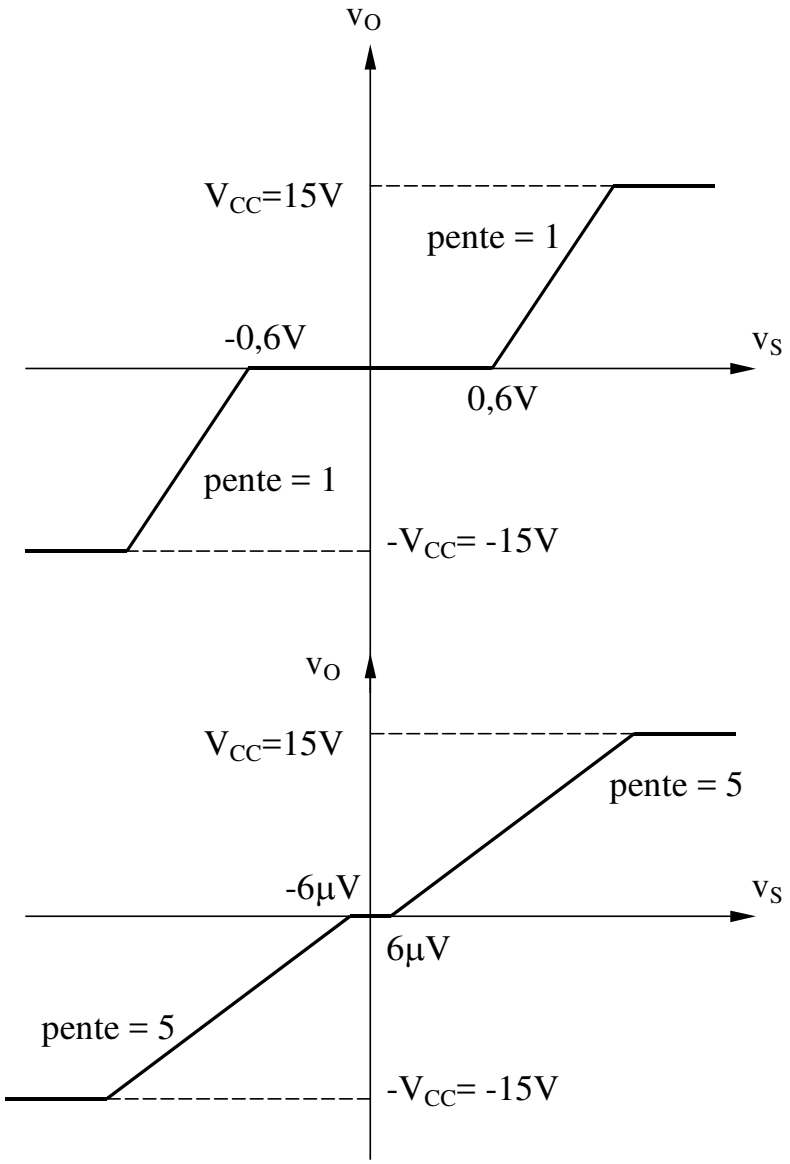

4.5. Class AB output stage

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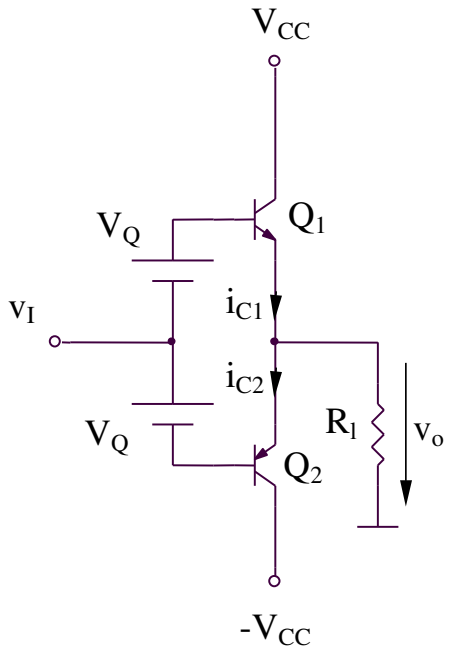
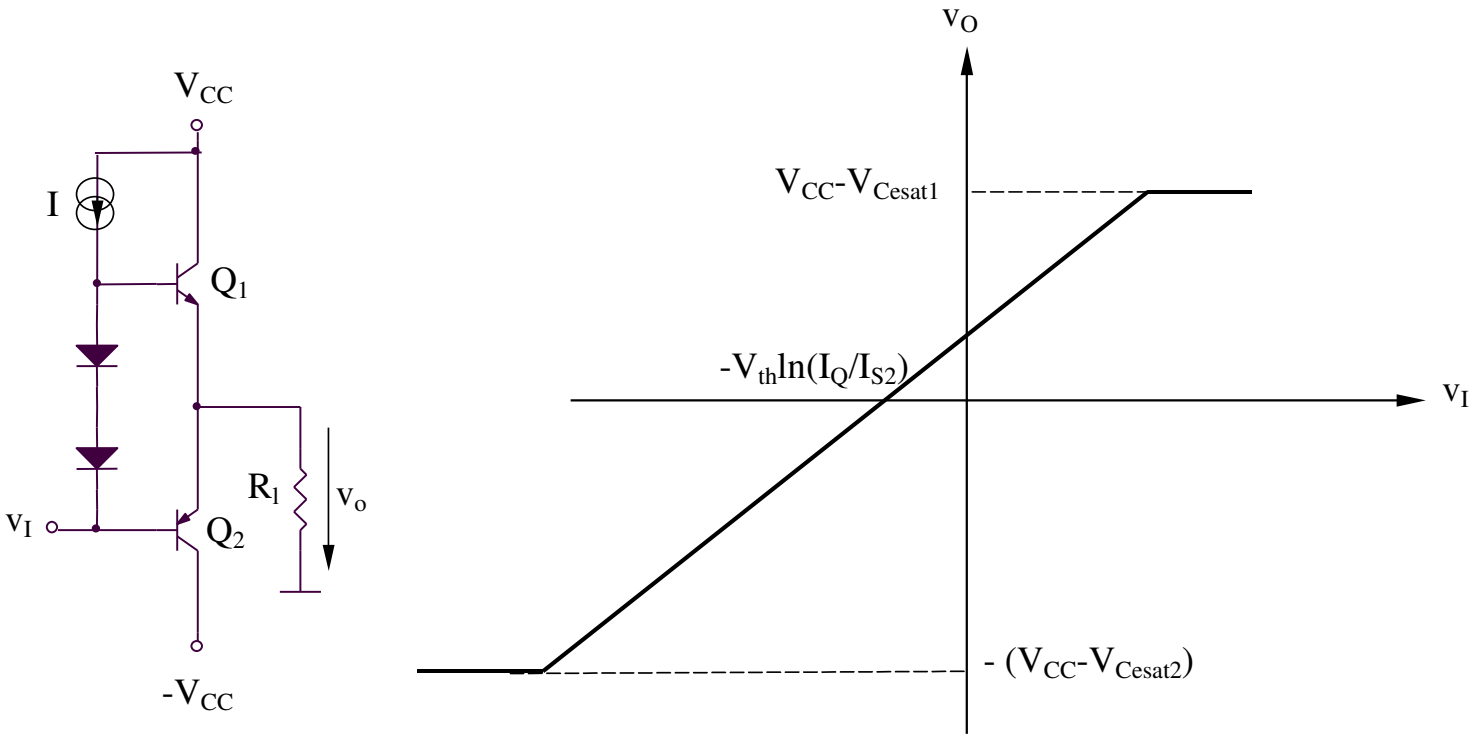


In order to obtain a good linearity of the global transfer characteristic, it is necessary to:
- have a good matching between the transistors from the circuit
- proper choose of biasing voltage in repose
- choose a pre-biasing of the output stage in order to avoid the thermal embalmment

Circuit for avoiding the thermal embalmment (1)

The biasing voltage of the output stage must be a temperature-dependent voltage (for example, the base-emitter voltage)

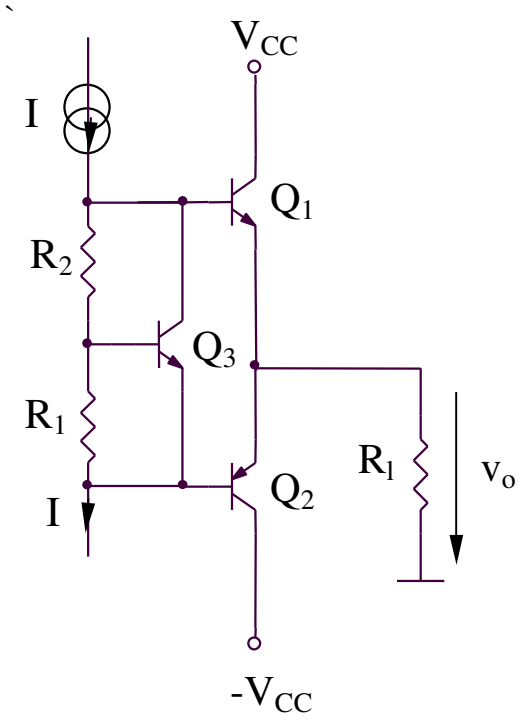


The diode-connected transistors must be at the same temperature with the final transistors. In repose :

$$v_O = 0 \Rightarrow I_{QC1} = I_{QC2} = I_Q$$

$$V_{BE1} + V_{EB2} = 2V_D \Rightarrow V_{th} \ln\left(\frac{I_Q}{I_{S1}}\frac{I_Q}{I_{S2}}\right) = 2V_{th}\ln\left(\frac{I}{I_{SD}}\right) \Rightarrow I_Q = I\frac{\sqrt{I_{S1}I_{S2}}}{I_{SD}}$$

Circuit for avoiding the thermal embalmment (2)

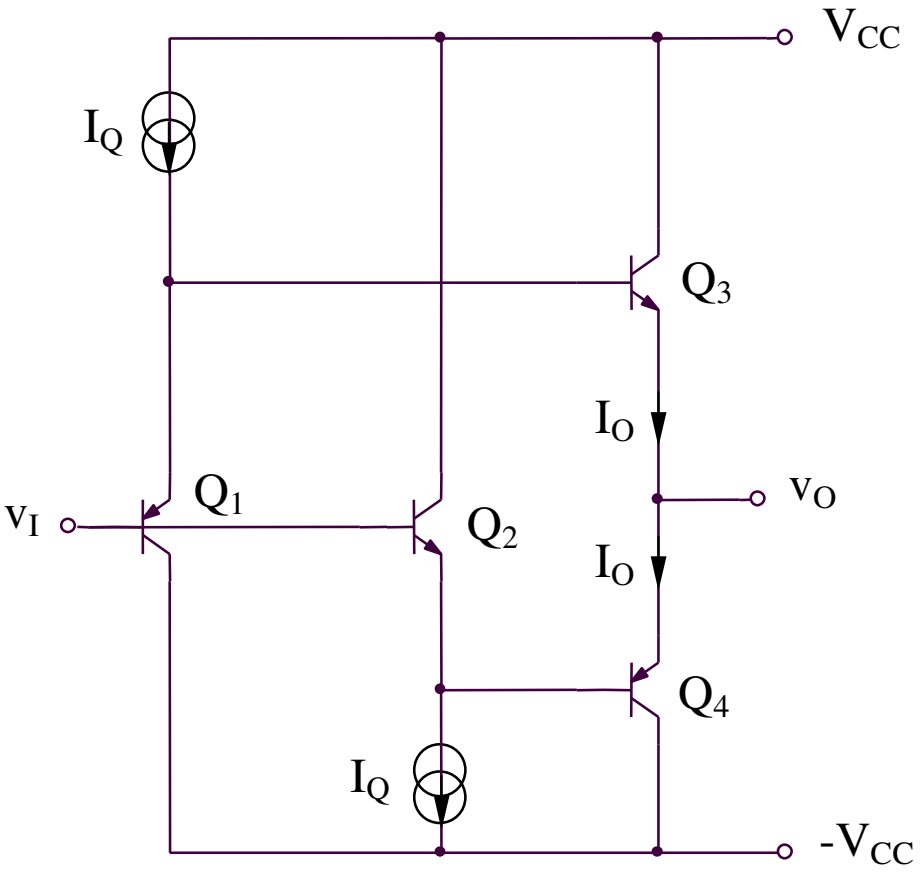


$$\left.\begin{aligned} v_{BE1} + v_{EB2} &= v_{CE3} \\ v_{CE3} &= \frac{v_{BE3}}{R_1}\left(R_1 + R_2\right) \end{aligned}\right\} \Rightarrow$$

$$\Rightarrow V_{th}\left(\ln\frac{I_Q}{I_{S1}} + \ln\frac{I_Q}{I_{S2}}\right) = \left(1 + \frac{R_2}{R_1}\right)V_{th}\ln\frac{I}{I_{S3}}$$

$$\Rightarrow I_Q = \sqrt{I_{S1}I_{S2}\left(\frac{I}{I_{S3}}\right)^{1+\frac{R_2}{R_1}}}$$

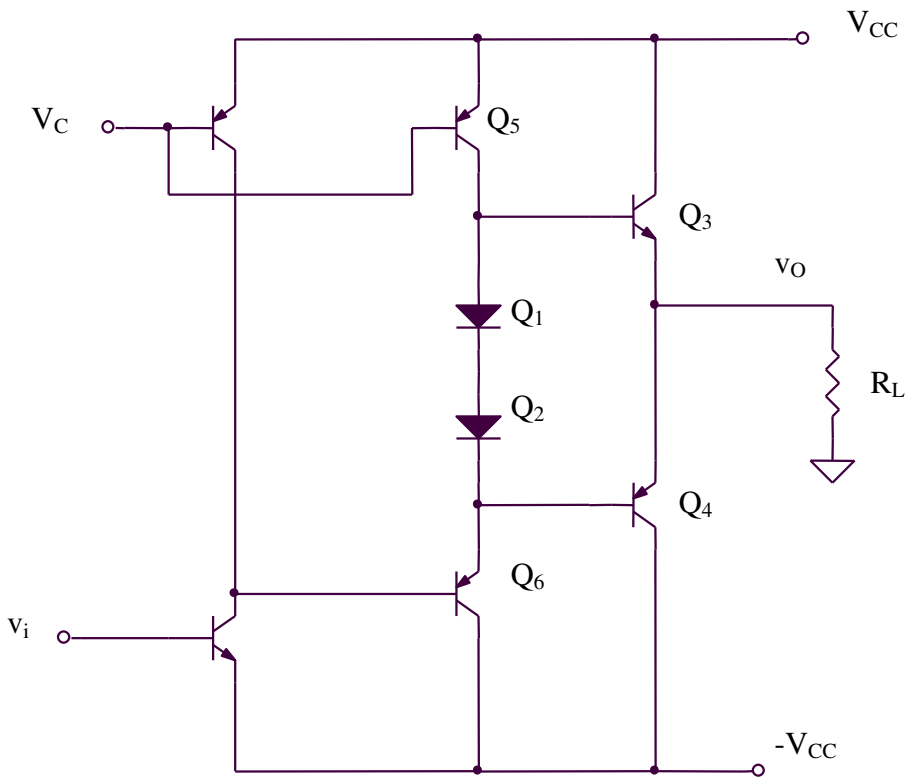
Circuit for avoiding the thermal embalmment (3)



$$/V_{BE1}/+V_{BE2}=V_{BE3}+/V_{BE4}/$$

$$2V_{th}\ln\frac{I_Q}{I_S}=2V_{th}\ln\frac{I_O}{I_S}\Rightarrow I_O=I_Q$$

Circuit for avoiding the thermal embalmment (4)



$$V_{BE1} + V_{BE2} = V_{BE3} + V_{EB4}$$

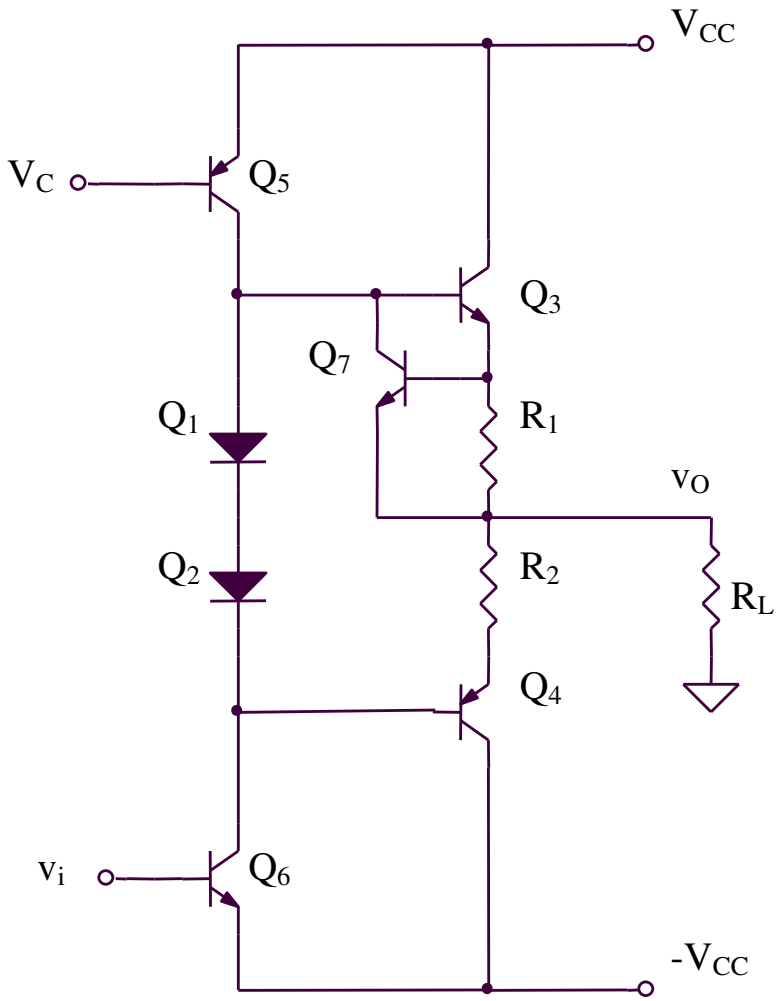
$$V_{th} \ln \frac{I_{C1}}{I_{S1}} + V_{th} \ln \frac{I_{C2}}{I_{S2}} = V_{th} \ln \frac{I_{C3}}{I_{S3}} + V_{th} \ln \frac{I_{C4}}{I_{S4}}$$

$$\Rightarrow I_{C3} = I_{C4} = I_{C1} \sqrt{\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}}$$

$$V_{O\,max}^{+} = V_{CC} - V_{EC5\,sat} - V_{BE3}$$

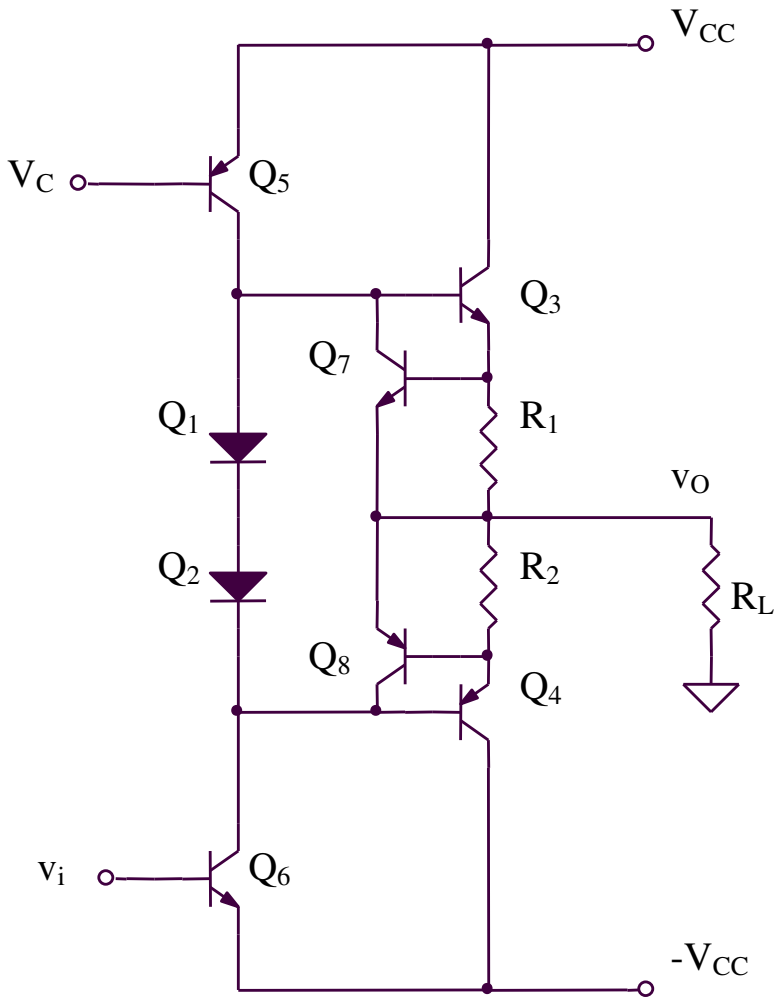
$$V_{O\,max}^{-} = -V_{CC} + V_{EC6\,sat} - V_{BE4}$$

Circuit with overload protection (1)



$$I_{O\,max}^{+} = \frac{V_{BE7}}{R_1}$$

Circuit with overload protection (2)



$$I_{O\,max}^{+} = \frac{V_{BE7}}{R_1}$$

$$I_{O\,max}^{-} = \frac{V_{EB8}}{R_2}$$