The Bipolar Junction Transistor

1. Introduction

The discovery of the Bipolar Junction Transistor (BJT) opened the era of modern electronics. William Shockley started in 1945 to begin organizing a solid-state physics group at Bell Labs. Among other things, this group pursued research on semiconductor replacements for unreliable vacuum tubes and electromechanical switches then used in the Bell Telephone System. In 1946, theoretical physicist John Bardeen suggested that electrons on the semiconductor surface might be blocking penetration of electric fields into the material, negating any effects. With experimental physicist Walter Brattain, Bardeen began researching the behavior of these "surface states." On December 16, 1947, their research culminated in the first successful semiconductor amplifier. Bardeen and Brattain applied two closely-spaced gold contacts held in place by a plastic wedge to the surface of a small slab of high-purity germanium. The voltage on one contact modulated the current flowing through the other, amplifying the input signal up to 100 times. On December 23, 1947, they demonstrated their device to lab officials - in what Shockley deemed "a magnificent Christmas present." Named the "transistor" by electrical engineer John Pierce, Bell Labs publicly announced the revolutionary solid-state device at a press conference in New York on June 30, 1948. A spokesman claimed that "it may have far-reaching significance in electronics and electrical communication." Despite its delicate mechanical construction, many thousands of units were produced in a metal cartridge package as the Bell Labs "Type A" transistor.

Fig.1. A replica of the first point-contact germanium transistor, Bell Labs (Lucent-Nokia)

In January 1948, William Shockley began a month of intense theoretical activity. On January 23, 1948 he conceived a distinctly different transistor based on the p-n junction discovered by Russell Ohl in 1940. Partly spurred by professional jealousy, as he resented not being involved with the point-contact discovery, Shockley also recognized that its delicate mechanical configuration would be difficult to manufacture in high volume with sufficient reliability. Shockley also disagreed with Bardeen's explanation of how their transistor worked. He claimed that positively charged holes could also penetrate through the bulk germanium material - not only trickle along a surface layer. Called "minority carrier injection," this phenomenon was crucial to operation of his junction transistor, a three-layer sandwich of n-type and p-type semiconductors separated by p-n junctions. This is how all "bipolar" junction transistors work today. On February 16, 1948, physicist John Shive achieved transistor action in a sliver of germanium with point contacts on opposite sides, not next to each other, demonstrating that holes were indeed flowing through the germanium. Shockley applied for a patent on the junction transistor that June and published his detailed theory of its operation in 1949.
The bipolar junction transistors are widely used today as discrete components or inside the analog or some digital integrated circuits, performing simple or complex electronic functions in electronic equipment.

2. **BJT brief theory**

Currently, the Bipolar Junction Transistors (BJT's) are manufactured on a large scale. They are the dominant components in radiofrequency and audio equipment. The basic material used to produce these transistors is silicon.
The BJT is a three terminal device which presents three doped regions: emitter, base, and collector (Fig.2). These regions form two p-n junctions between them. The emitter has a moderate size and it is heavily doped causing it to supply a large number of carriers for the flow of current. The base is thin and lightly doped. The collector is larger than the emitter (wide) and is moderately doped. Hence, it collects most of the majority carriers supplied by the emitter.

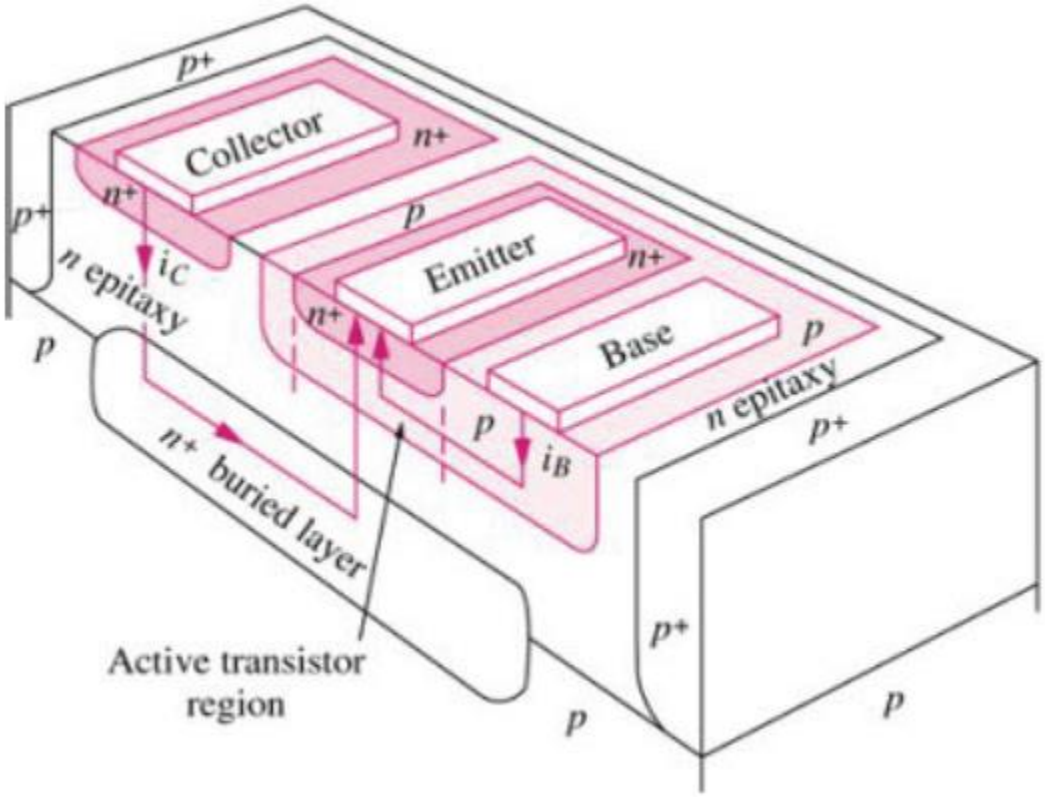


Fig.2.The internal structure of a npn bipolar junction transistor

Depending on the impurities introduced into the silicon in the manufacturing process, there are 2 types of bipolar junction transistors: the npn BJT and the pnp BJT. Thus, two types of charge carriers will circulate through a device: electrons and holes (Fig.3). For this reason the BJT's are called bipolar devices. Most circulating charge carriers through the semiconductor material are the holes for the pnp transistor and the electrons for the npn transistor. Because the mobility of electron is greater than the mobility of the hole, the npn transistor has a faster response time compared to a pnp transistor. Therefore, in practice npn transistors are more widespread than the pnp transistors.

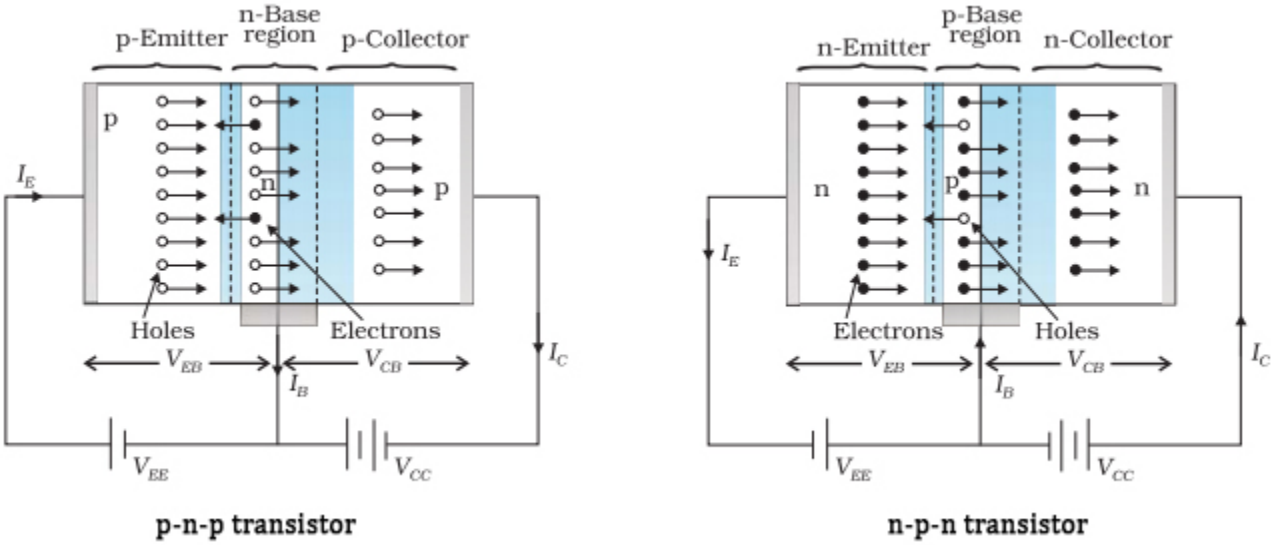


Fig.3.The charge flow through bipolar junction transistor biased in the forward active region

The symbols for the npn and pnp bipolar junction transistors are represented in Fig.4. The terminals can be identified by consulting the part datasheet given by the manufacturer.

Fig.4.The electrical symbol for the bipolar junction transistor: a) n-p-n BJT; b) p-n-p BJT
The terminals are: C-Collector; B-Base; E-Emitter

Since it has three terminals, the bipolar junction transistor can be described by using six electrical parameters (Fig.5):

- three currents (i_B: the base current; i_C: the collector current; i_E: the emitter current);
- and three voltages (v_{BE}: the base-emitter voltage; v_{BC}: the base-collector voltage; v_{CE}: the collector-emitter voltage).

The Kirchhoff's circuit laws may be written for the bipolar junction transistor:

$$i_E = i_C + i_B \tag{1}$$

$$v_{CE} = v_{BE} + v_{CB} = v_{BE} - v_{BC} \tag{2}$$

Thus, only four of these 6 parameters are independent parameters: i_C, i_B, v_{BE}, v_{CE}.

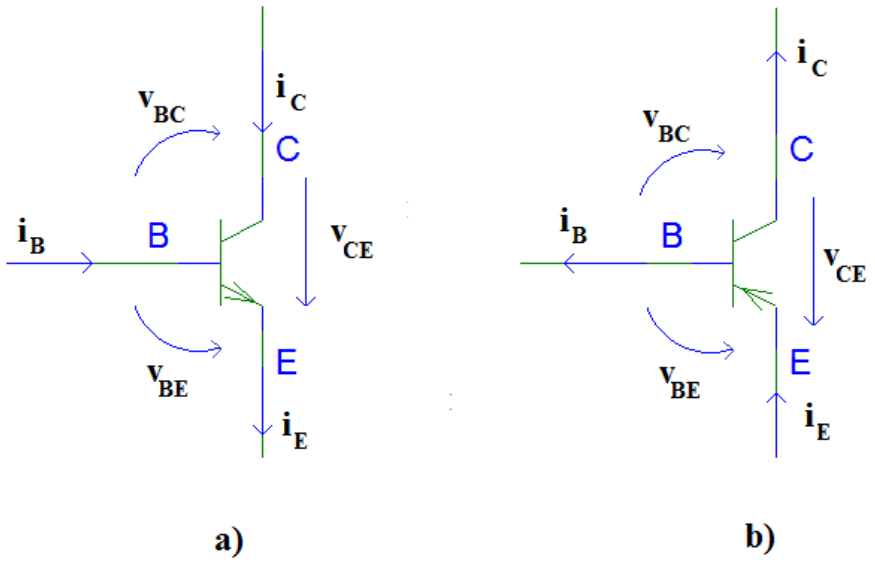


Fig.5.The electrical parameters which define the state of the bipolar junction transistor: a) n-p-n BJT; b) p-n-p BJT. The terminals are: C-Collector; B-Base; E-Emitter

1. *BJT junctions measurement*

The BJT can be viewed (Fig.3) as a structure of two pn junctions placed back to back. It is very important to understand that the transistor effect occurs in a single silicon crystal and that the device cannot be built using two interconnected pn junctions (which are built of two different silicon crystals). To check the two junctions of the BJT, an analog ohm-meter can be used (e.g. Simpson 260, MAVO 35), by connecting it in turn to each of the junctions (Fig.6). The third terminal of the device (unused) can be left unconnected (in the air). The indication of the ohm-meter should be about halfway for base-emitter and base-collector junctions when they are in forward bias (the ohm-meter has a 1.5V internal battery and the voltage drop on the transistor junction is about 0.6V). In reverse bias, when the ohm-meter is connected to the base-emitter and base-collector junctions, the indicator needle should not move (infinite resistance). Also, when measuring the collector-emitter junction, the analog ohm-meter must indicate an infinite resistance.

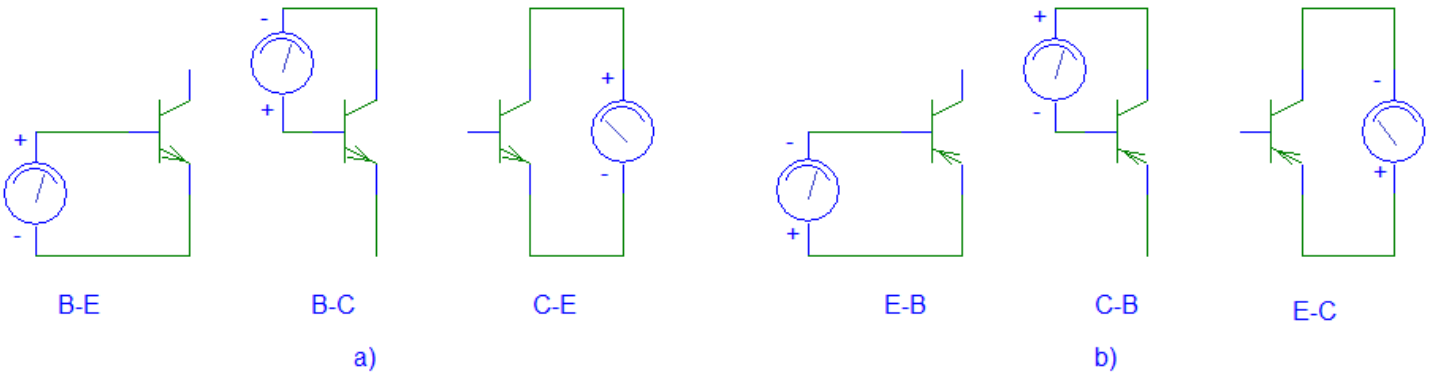


Fig. 6.The measurement of the BJT junction by using an ohm-meter: a) npn BJT; b) pnp BJT

2. *BJT operating regimes*

The BJT operation is based on changing the collector current (i_C) as a function of the bias current injected into the base terminal (i_B), so it is a current controlled device. Since the BJT has 2 internal pn junctions (and one pn junction has two bias regimes-*forward bias and reverse bias*-), it results that the transistor will have four operating regimes: forward-active, saturation, cut-off and reverse active (*Table 1*).

Table 1- Operating regimes for BJT (approximate data)

Transistor type	Operating regime	Junction bias		Junction voltage polarity
		BE junction	BC junction	
NPN	forward-active	forward bias	reverse bias	$v_{BE}>0$, $v_{BC}<0$
	saturation	forward bias	forward bias	$v_{BE}>0$, $v_{BC}>0$
	cut-off	reverse bias	reverse bias	$v_{BE}<0$, $v_{BC}<0$
	reverse-active	reverse bias	forward bias	$v_{BE}<0$, $v_{BC}>0$
PNP	forward-active	forward bias	reverse bias	$v_{BE}<0$, $v_{BC}>0$
	saturation	forward bias	forward bias	$v_{BE}<0$, $v_{BC}<0$
	cut-off	reverse bias	reverse bias	$v_{BE}>0$, $v_{BC}>0$
	reverse-active	reverse bias	forward bias	$v_{BE}>0$, $v_{BC}<0$

The bias regimes for a npn transistor are presented in Fig.7. In a similar way the bias regimes for a pnp transistor can be represented, too.

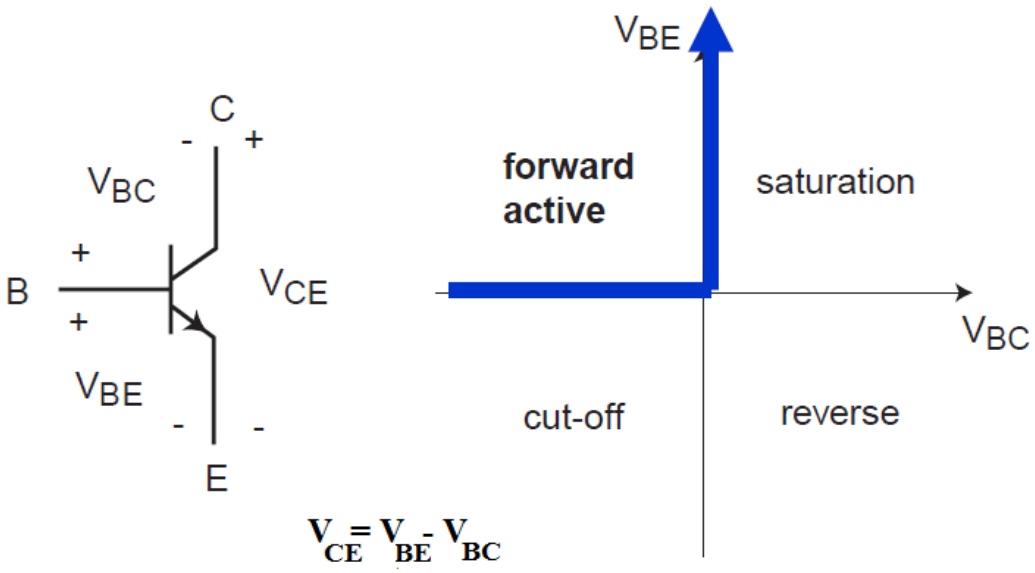


Fig.7. A simplified graph with the operating regimes for the npn BJT

3. The forward-active regime

The most used bias regime for the BJT is the forward-active regime, because in this regime the transistor can be used as amplifier, to amplify the AC signals. The BJT operation assumes that DC voltages are present between both BE and CE terminals. Given the roughly data presented in Table 1, the conditions that must be met by the bias voltages which are applied to the transistor terminals to be in the forward active regime are refined in *Table 2*.

Table 2- The bias of the BJT junctions in the forward-active regime

Transistor type	Bias conditions
NPN	$v_{BE} \in \left[V_{\gamma}; V_{BEsat}\right]; V_{CEsat} \le v_{CE} \le V_{(BR)CEO}\ ;\ -V_{(BR)CBO} \le v_{BC} \le v_{BE} - V_{CEsat}$
PNP	$v_{EB} \in \left[V_{\gamma}; V_{EBsat}\right]; V_{ECsat} \le v_{EC} \le -V_{(BR)CEO}; V_{(BR)CBO} \le v_{CB} \le v_{EB} - V_{ECsat}$

The introduced parameters are:

- V_γ represents the opening voltage of the base-emitter junction in forward bias (typically between *0.2÷0.5V*), and it is the maximum base-emitter voltage where I_B~0;
- V_{BEsat} is the base-emitter saturation voltage (≈0.7V÷0.8V);
- V_{CEsat} is the collector-emitter saturation voltage (≈0.1V÷0.5V);
- $V_{(BR)CEO}$ is the collector-emitter breakdown voltage;
- $V_{(BR)CBO}$ is the collector-base breakdown voltage.

Over the DC signal applied to the transistor, the AC signal is superimposed, usually with smaller amplitude.

The BE junction is typically a pn junction and it acts like a diode. When this junction is forward biased, there are two currents passing through the junction: an important current provided by the electrons (for npn transistor) or holes (for pnp transistor) (Fig.3) which flow from emitter to the base, and a small current of holes (for npn transistor) or electrons (for pnp transistor) from the base to the emitter. The base width is small, and when a voltage is applied between the collector and the emitter, most of the electrons (npn transistor) or holes (pnp transistor) that were moving from emitter to base, cross the thin base region and they are collected at the collector region. The BC junction is in reverse bias. Because the base width is small, a large current flow through this region (electrons for npn transistor, holes for pnp transistor). The amount of the current that crosses from emitter to collector region depends strongly on the voltage applied to the BE junction, v_{BE} (it also depends weakly on voltage applied between collector and emitter, v_{CE}). As such, small changes in v_{BE} or i_B controls a much larger collector current i_C. Note that the transistor does not generate i_C. It acts as a valve controlling the current that can flow through it. The source of current (and power) is the power supply that feeds the CE terminals. The transistor effect means that the carriers injected from the emitter (electrons for npn type transistor, holes for pnp type transistor) to the base are extracted by the collector.

The collector current is:

$$I_C = I_S \cdot \exp\left(\frac{V_{BE}}{V_{th}}\right)\left(1+\frac{V_{CE}}{V_A}\right) \tag{3}$$

,where:

- I_S is the BJT saturation current (different from pn junction I_S);
- $V_{th} = \frac{k \cdot T}{q}$ is the thermal voltage (about 26mV at 300K) with k – the Boltzmann's constant, q- the elementary electrical charge ($1.6 \cdot 10^{-19}$C) and T- the absolute temperature;
- V_A is the Early voltage (typically between 60V and 100V for a low power BJT).

The DC current gain is:

$$\beta_F = \frac{I_C}{I_B} \tag{4}$$

,where:

- I_C is the DC collector current;
- I_B is the DC base current.

β_F is is a dimensionless physical quantity that that can have typical values between 10 and 1000, and it is replaced in the device datasheet by the hybrid parameter h_{FE}:

$$h_{FE} = \beta_F \tag{5}$$

The characteristic $i_C=f(v_{BE})$ for a low power npn BJT used in low frequency amplifiers (below 1MHz), in a common emitter configuration, at three different Early voltages ($V_{A1}>V_{A2}>V_{A3}$), is represented in Fig.8.

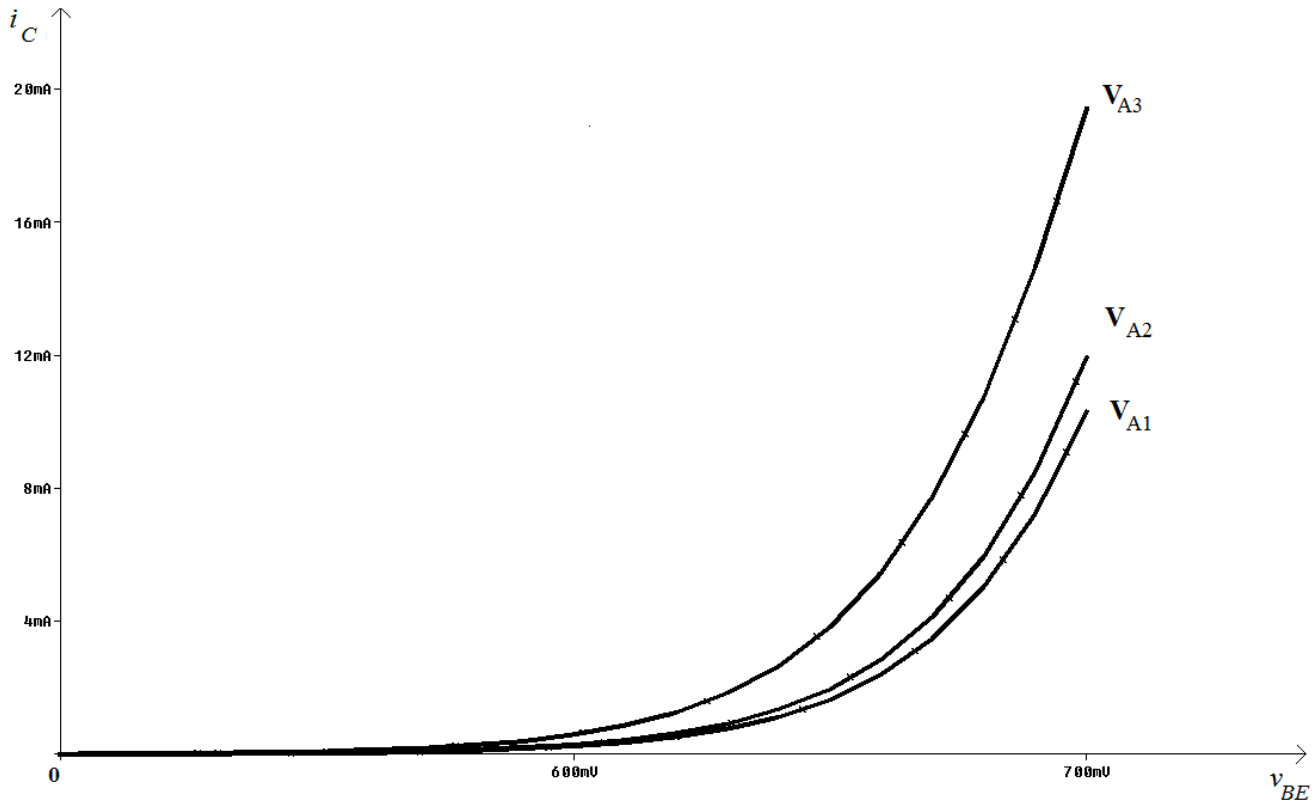


Fig.8.The transfer characteristic $i_C=f(v_{BE})$ for a low power npn-BJT when changing the Early voltage

Temperature influence

When the ambient temperature changes, it will influence the following parameters: the saturation current (I_S), the base-emitter voltage (V_{BE}), and the thermal voltage (V_{th}).

The saturation current is:

$$I_S = \frac{q \cdot A_E \cdot D_n \cdot n_i^2}{N_B \cdot W_B} \tag{6}$$

,where:

- A_E is the emitter area;
- D_n is the diffusion constant for electrons;
- n_i is the intrinsic carrier concentration;
- N_B is the base doping concentration;
- W_B is the width of the base region.

Two of the mentioned parameters are strongly influenced by temperature:

$$D_n = \frac{k \cdot T}{q} \cdot \mu_n = \frac{k \cdot T}{q} \cdot C \cdot T^{-n} \tag{7}$$

$$n_i^2 = D \cdot T^3 \cdot \exp\left(-\frac{q \cdot V_{G0}}{k \cdot T}\right) \tag{8}$$

,where:

- μ_n is the mobility of electrons;
- C and D are constants (independent with temperature);
- V_{G0} is the band gap of Si at absolute 0.

By replacing in (6), it results:

$$I_S = \frac{q \cdot A_E}{N_B \cdot W_B} \cdot \left(\frac{k \cdot T}{q} \cdot C \cdot T^{-n} \right) \cdot D \cdot T^3 \cdot \exp\left(-\frac{q \cdot V_{G0}}{k \cdot T} \right) \tag{9}$$

$$I_S = \frac{k \cdot A_E}{N_B \cdot W_B} \cdot C \cdot D \cdot T^{4-n} \cdot \exp\left(-\frac{q \cdot V_{G0}}{k \cdot T} \right) \tag{10}$$

By neglecting the Early effect, the V_{BE} voltage may be determined from Eq(3):

$$V_{BE}(T) = V_{th} \cdot \ln\left(\frac{I_c}{I_S} \right) = \frac{k \cdot T}{q} \cdot \ln\left(\frac{I_c}{I_S} \right) \tag{11}$$

By replacing the saturation current, it results:

$$V_{BE}(T) = \frac{k \cdot T}{q} \cdot \ln\left(\frac{I_c}{\frac{k \cdot A_E}{N_B \cdot W_B} \cdot C \cdot D \cdot T^{4-n} \cdot \exp\left(-\frac{q \cdot V_{G0}}{k \cdot T} \right)} \right) \tag{12}$$

$$V_{BE}(T) = V_{G0} + \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_B \cdot W_B}{k \cdot A_E \cdot C \cdot D} \cdot I_c \cdot T^{n-4} \right) \tag{13}$$

$$V_{BE}(T) = V_{G0} + \frac{k \cdot T}{q} \cdot \ln\left(ct \cdot I_c \cdot T^{n-4} \right) \tag{14}$$

, where *ct* is a constant:

$$ct = \frac{N_B \cdot W_B}{k \cdot A_E \cdot C \cdot D} \tag{15}$$

It results:

$$\frac{V_{BE}(T) - V_{G0}}{T} = \frac{k}{q} \cdot \ln\left(ct \cdot I_c \cdot T^{n-4} \right) \tag{16}$$

By calculating the first derivative of Eq. (14), we obtain:

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \cdot \ln\left(I_C \cdot ct \cdot T^{n-4} \right) - \frac{k \cdot T}{q} \cdot \left(\frac{1}{I_C \cdot ct \cdot T^{n-4}} \right) \cdot (4-n) \cdot I_C \cdot ct \cdot T^{n-3} \tag{17}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \cdot \ln\left(I_C \cdot ct \cdot T^{n-4} \right) - \frac{k}{q} \cdot (4-n) \tag{18}$$

From Eqs. (16÷18) it results:

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE}(T) - V_{G0}}{T} - \frac{k}{q} \cdot (4-n) \tag{19}$$

At room temperature, for a silicon transistor, the value for this derivative is approximately:

$$\frac{\partial V_{BE}}{\partial T} \cong -2mV / K \tag{20}$$

The characteristic $i_C = f(v_{BE})$ for a npn BJT used as a common emitter amplifier at three different working temperatures ($T3 > T2 > T1$) is represented in Fig.9. The increase in current is very large as the temperature increases, when the base-emitter voltage remains constant. This may cause the device to heat up, and through the device there will be an additional increase in current due to this heating. The temperature acts on the device as a positive feedback circuit. In some cases the destruction of the junctions may occur if no current limiting measures are taken.

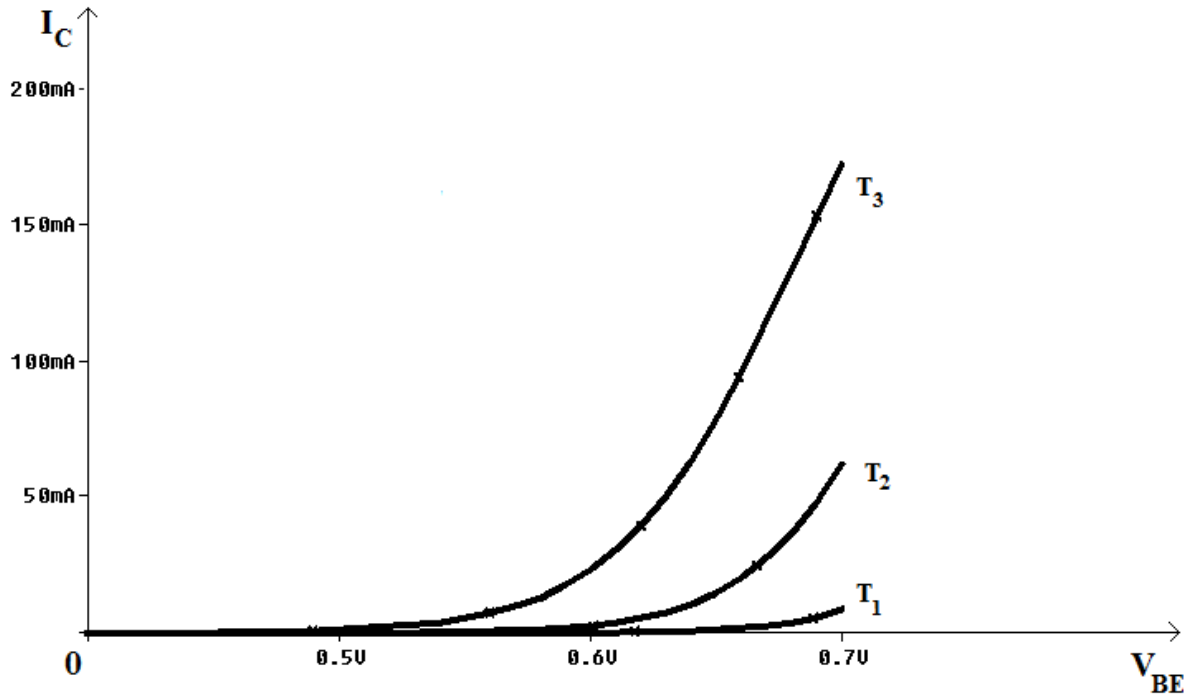


Fig.9.The transfer characteristic $i_C=f(v_{BE})$ for a low power npn-BJT when changing the temperature

The base current may be written as a function of the collector current and β (we neglected the Early effect):

$$I_B = \frac{I_C}{\beta_F} = \frac{I_S}{\beta_F} \cdot \exp\left(\frac{V_{BE}}{V_{th}}\right) \tag{21}$$

The input characteristic for a npn BJT ($I_B=f(V_{BE})$) biased in the forward active regime is represented in Fig.10, and it is similar to the pn junction characteristic in the forward bias regime.

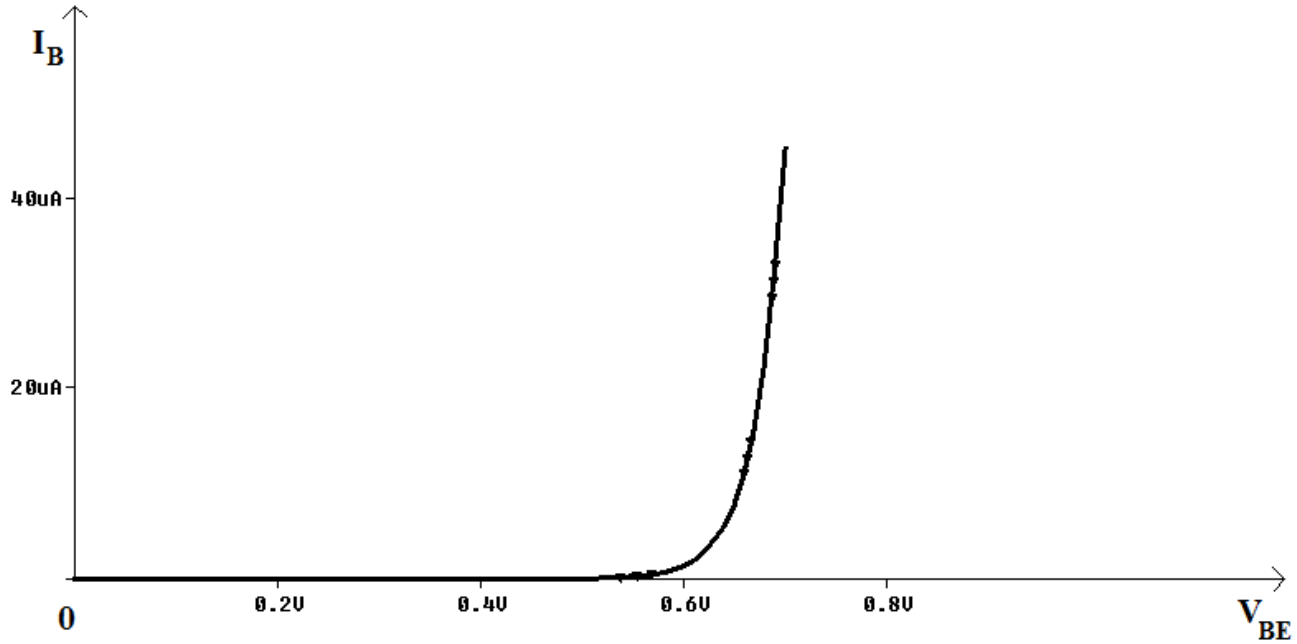


Fig.10.The input characteristic $I_B=f(V_{BE})$ for a low power npn-BJT

The transfer characteristic $I_c=f(I_B)$ for a low power npn bipolar junction transistor. The parameter β_F can be extracted from this graph.

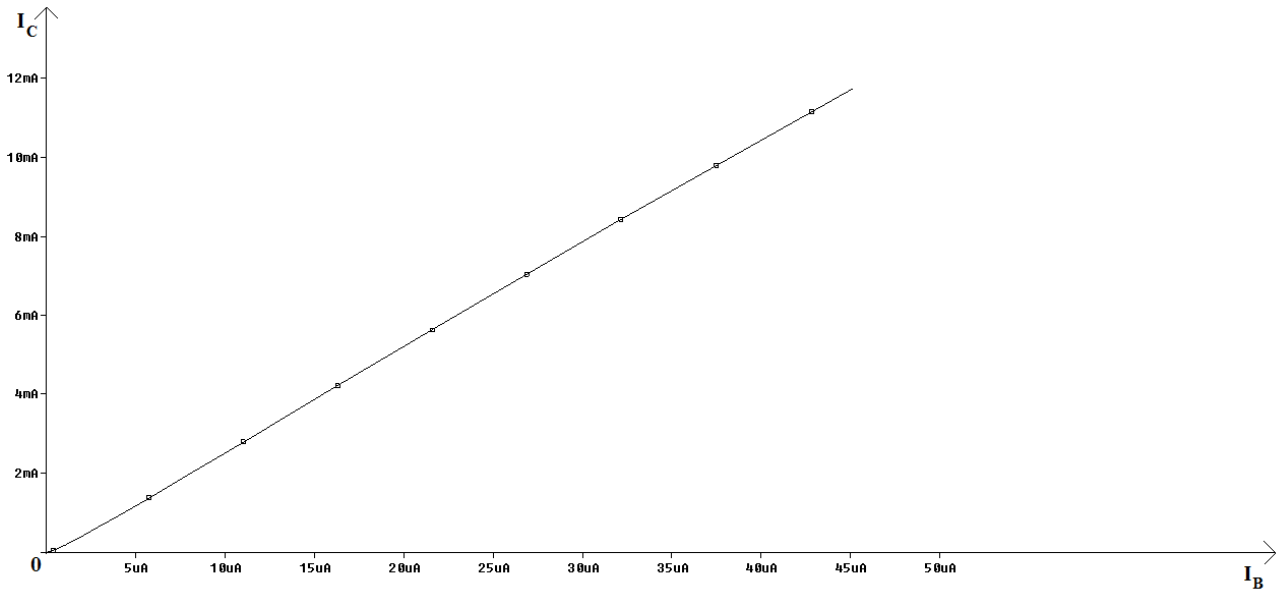


Fig.11.The transfer characteristic $I_c=f(I_B)$ for a low power npn-BJT

The output characteristics $Ic=f(V_{CE})$ for a npn bipolar junction transistor used in a common emitter configuration amplifier at different base-emitter voltages ($V_{BE1}< V_{BE2}< V_{BE3}< V_{BE4}< V_{BE5}< V_{BE6}$) are represented in Fig.12. The slope of the current-voltage characteristic in the forward active region is given by the influence of the Early voltage.

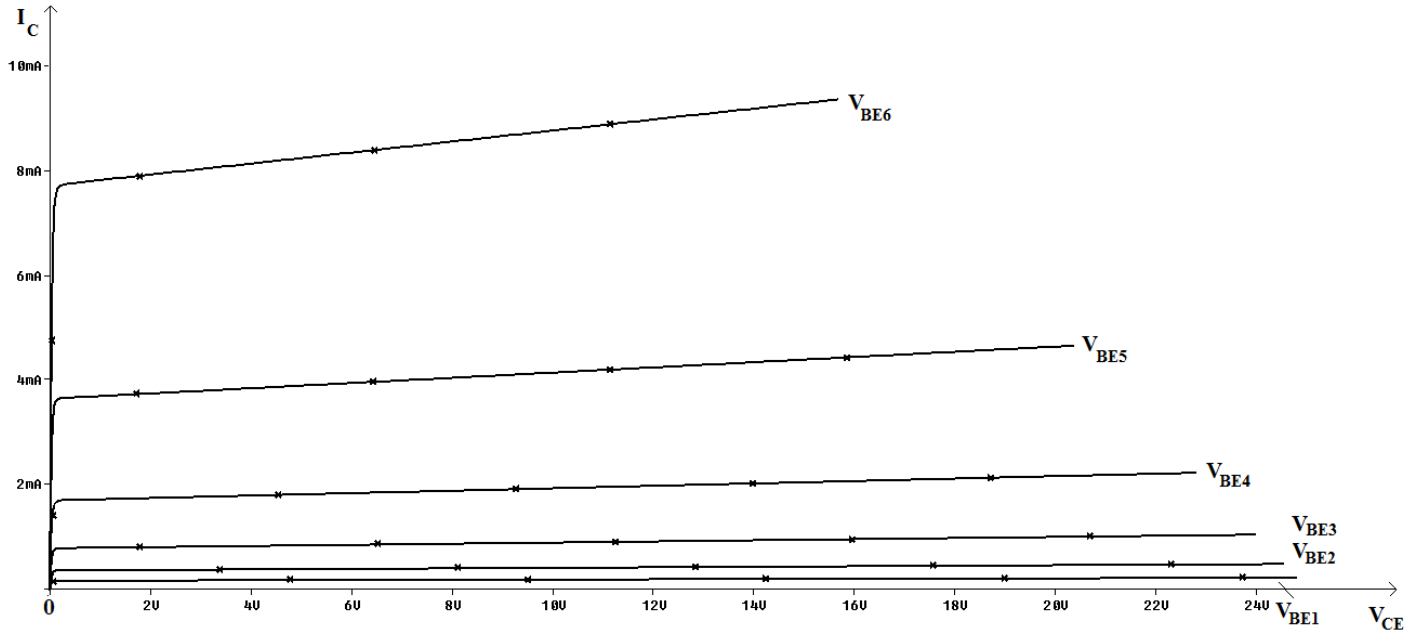


Fig.12.The output characteristic $I_c=f(V_{CE})$ for a low power npn-BJT

4. The saturation regime

In the saturation regime, both junctions are forward biased, and the base and the collector currents may attain the highest values (*Table 3*).

Table 3- The bias of the BJT junctions in the saturation regime

Transistor type	Bias conditions
NPN	$v_{BE} \in \left[V_{BEsat}; V_{BEsat\max}\right];\ 0 \le v_{CE} \le V_{CEsat}\ ;\ V_{BEsat} - V_{CEsat} \le v_{BC} \le V_{BEsat\max}$
PNP	$v_{EB} \in \left[V_{EBsat}; V_{EBsat\max}\right]; 0 \le v_{EC} \le V_{ECsat}\ ; V_{EBsat} - V_{ECsat} \le v_{CB} \le V_{EBsat\max}$

The parameter $V_{BEsat\max}$ is the maximum base-emitter voltage in the saturation regime (typically 1V÷3V).

The transistor acts as a closed switch (it is considered in ON state in digital circuits, Fig.13).

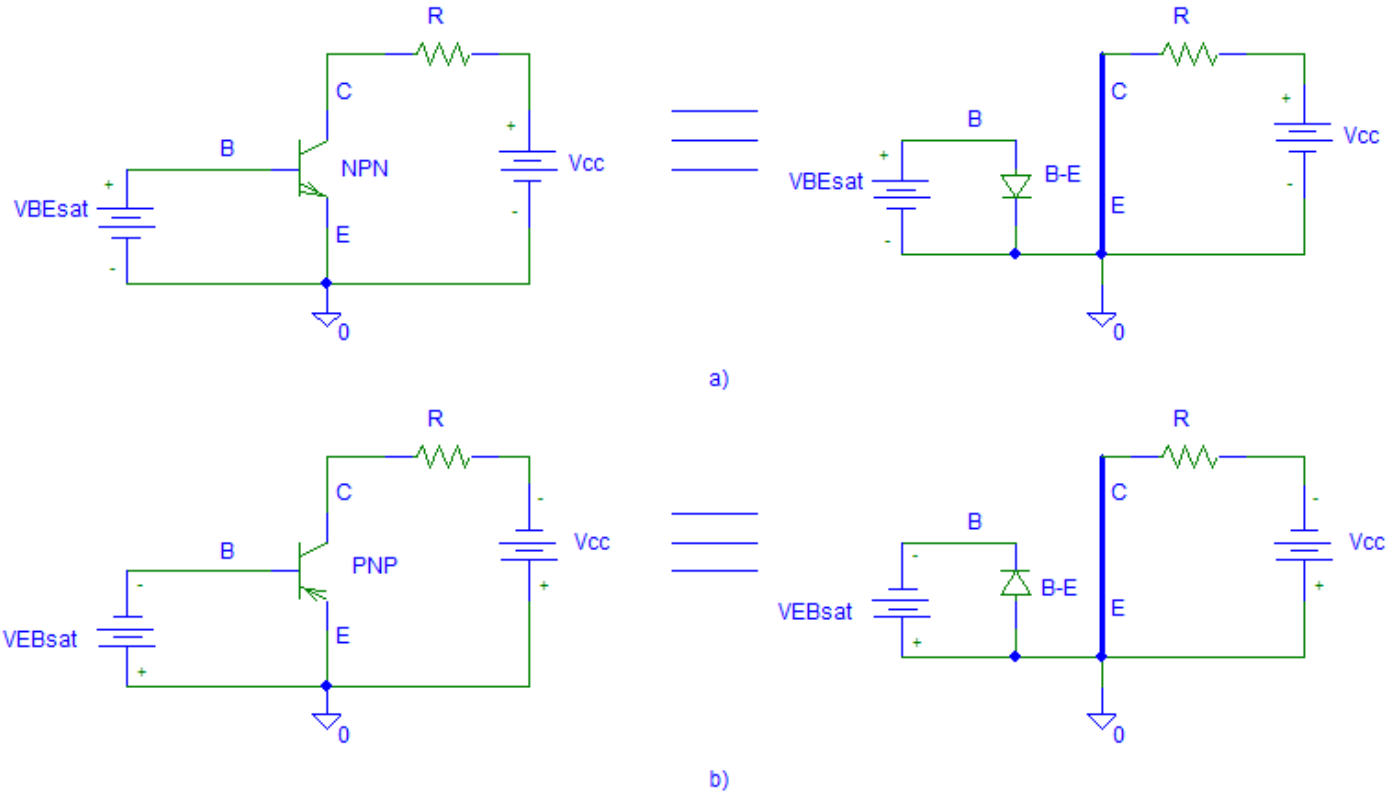


Fig.13.The equivalent circuit for a BJT used in digital circuits in the saturation regime: a) npn BJT; b) pnp BJT.

The transistor will be in the saturation if and only if:

$$\beta_F > \frac{I_C}{I_B} \tag{22}$$

The reason for this inequality is that both junctions are injecting and collecting charges (and the base current in the saturation regime is much higher compared to the base current in the forward active regime).

For the npn transistor, the following physical mechanisms occur:

- electrons are injected from emitter into base and they are collected by the collector;
- electrons injected from collector into the base are collected by the emitter;
- holes injected into emitter recombine at ohmic contact;
- holes injected into collector recombine with electrons in the n+ buried layer.

For the pnp transistor, there is the following situation:

- holes are injected from emitter into base and they are collected by the collector;
- holes injected from collector into the base are collected by the emitter;
- electrons injected into emitter recombine at ohmic contact;
- electrons injected into collector recombine with electrons in the p+ buried layer.

5. The cut-off regime

In the cut-off regime, both BJT junctions are in the reverse bias (*Table 4*). The base extracts charges (holes for the npn transistor, electrons for the pnp transistor) from the emitter and the collector regions.
The collector current is given by:

$$I_C = \frac{I_S}{\beta_R} = -I_{B1} \tag{23}$$

where β_R is the DC gain of the transistor in the reverse-active regime:

$$\beta_R = \frac{I_E}{I_B} \tag{24}$$

β_R is very small compared to β_F (it has typical values between 0.1 and 5).
The emitter current is:

$$I_E = \frac{I_S}{\beta_F} = -I_{B2} \tag{25}$$

The currents through the terminals of the transistor are very small (0.1fA for state of the art IC BJT's ÷ tens of nA for general purpose discrete BJT's), so they may approximated by zero.
The transistor acts as an open switch.

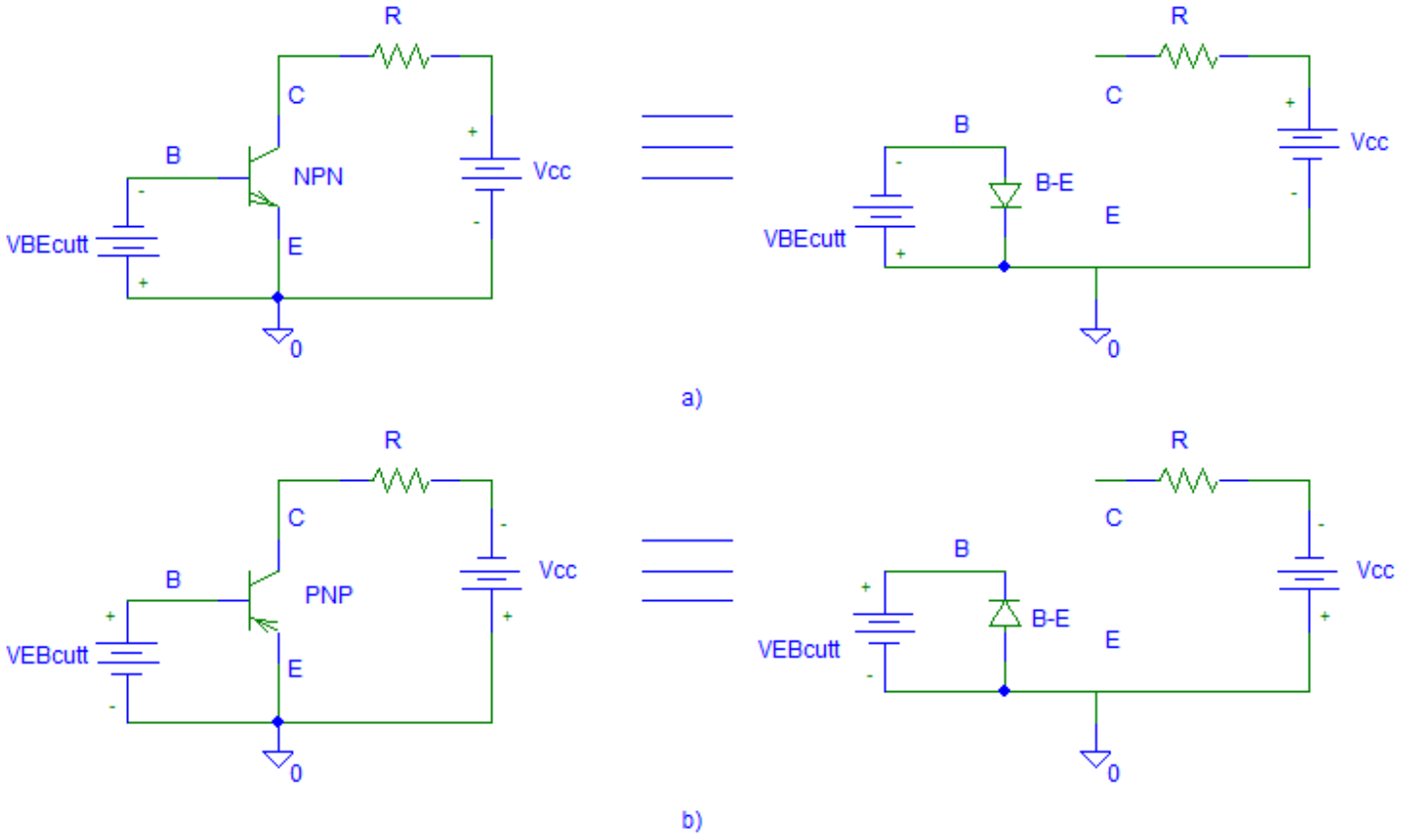


Fig.14.The equivalent circuit for a BJT in the cut-off regime: a) npn BJT; b) pnp BJT.

Table 4- The bias of the BJT junctions in the cut-off regime

Transistor type	Bias conditions
NPN	$v_{BE} \in \left[-V_{(BR)EBO}; V_{\gamma}\right];\ V_{CC} \approx v_{CE} \le V_{(BR)CEO}\ ;\ -V_{(BR)CBO} \le v_{BC} \le V_{\gamma} - V_{CC}$
PNP	$v_{EB} \in \left[V_{(BR)EBO}; V_{\gamma}\right]; V_{CC} \approx v_{EC} \le -V_{(BR)CEO}; V_{CC} - V_{\gamma} \le v_{BC} \le V_{(BR)CBO}$

The introduced parameters are:

- $V_{(BR)EBO}$ is the emitter-base breakdown voltage;
- V_{CC} is the supply voltage applied between collector and emitter (through some resistors);
- $V_{(BR)CEO}$ is the collector-emitter breakdown voltage;
- $V_{(BR)CBO}$ is the collector-base breakdown voltage.

6. The reverse-active regime

The reverse-active regime is rarely used. In this regime, the B-E junction is in the reverse bias, and the B-C junction is in forward bias (Table 5).

Table 5- The bias of the BJT junctions in the reverse-active regime

Transistor type	Bias conditions
NPN	$v_{BE} \in \left[-V_{(BR)EBO}; V_{\gamma}\right];\ V_{\gamma} \le v_{BC} \le V_{BC\max}$.
PNP	$v_{EB} \in \left[V_{(BR)EBO}; V_{\gamma}\right]; V_{\gamma} \le v_{CB} \le V_{CB\max}$.

The parameter $V_{BC\max}$ is the maximum voltage to be applied on the B-C junction (at this voltage the maximum allowable current will flow through the base, I_{Bmax}), and it may be approximated by the V_{BEsat} .

In the reverse-active regime:

- the collector injects charges (electrons for the npn transistor, holes for the pnp transistor) into the base and the emitter collects the charges (electrons for the npn transistor, holes for the pnp transistor) from the base;
- the base injects charges (holes for the npn transistor, electrons for the pnp transistor) into collector. These charges recombine at the collector contact and buried layer.

The DC gain in the reverse-active regime is:

$$\beta_R = \frac{I_E}{I_B} \in [0.1; 5] \tag{26}$$

The BJT small signal AC model at low frequencies

When the BJT is used as a small signal amplifier, an alternating voltage with amplitude less than the thermal voltage (V_{th}) is applied on the base-emitter junction. This allows an approximately linear response of the circuit in which the device is used. The transistor should be DC biased in the forward-active regime.

$$\underline{V_{be}} \ll V_{th} = \frac{k \cdot T}{q} \left(\approx 26mV \text{ at room temperature(300K)}\right) \tag{27}$$

The AC small signal model for low frequencies (below 10 KHz) of the BJT is given in Fig.15. The transconductance (g_m) and the input and the output resistances of the device (r_{be}, r_o) are:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_{th}} \approx 40 \cdot I_C \left(mA/V\right) \tag{28}$$

$$r_O = \frac{\partial V_{CE}}{\partial I_C} = \frac{V_A}{I_C}\left(k\Omega\right) \tag{29}$$

$$r_{be} = \frac{\beta_0}{g_m} \tag{30}$$

,where β_0 represents the AC current gain of the device:

$$\beta_0 = \frac{i_c}{i_b} \tag{31}$$

The output resistance may be neglected in some situations.

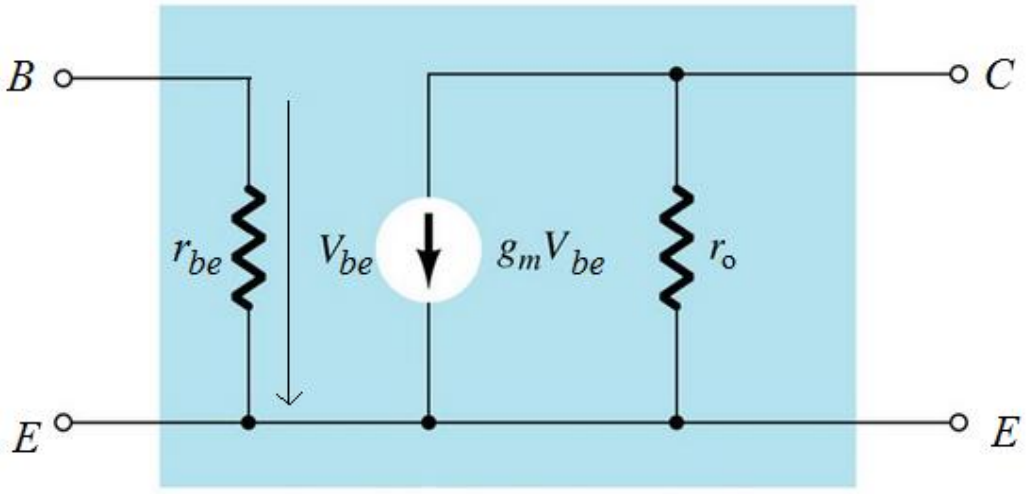


Fig.15.The AC equivalent circuit for the BJT

The common emitter amplifier

Consider the circuit from Fig. 16, which contains a npn bipolar junction transistor.

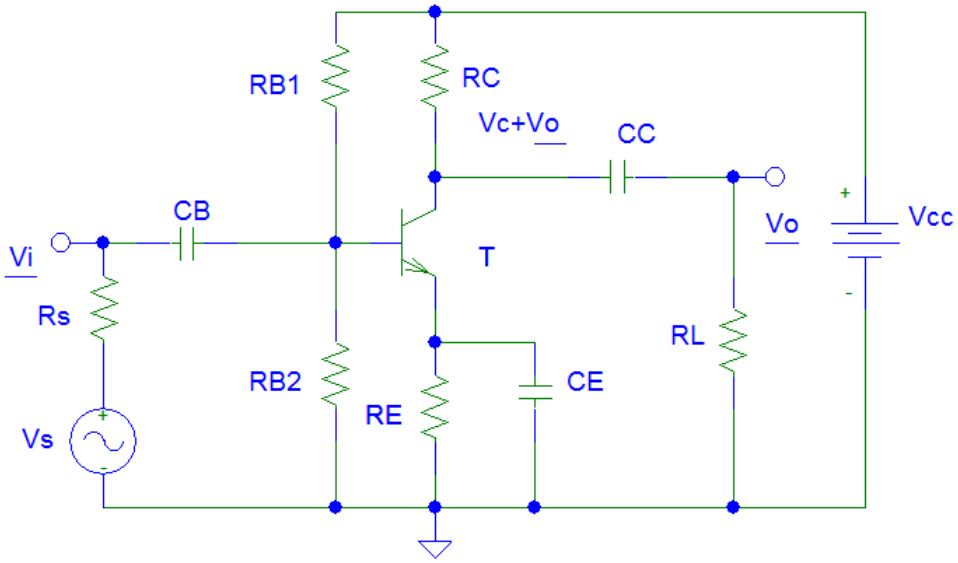


Fig.16.The npn BJT in a common emitter amplifier configuration

By using a set of resistors (R_{B1}-R_{B2} voltage divider, R_C and R_E), the device is biased from a single supply voltage (V_{CC}) in the forward active regime. The bias operating point for the BJT should be chosen wisely so as to avoid the entry of the device in the blocking regime or the saturation regime when the alternating current signal is superimposed over the direct current one.
In this circuit there are two coupling capacitors (C_B is used to connect the AC voltage source Vs to the base and to block the DC component to pass from the base to the AC voltage source, C_C is used to connect the collector to the external load resistor, R_L, and to block the DC component to pass from the collector to the load) and one decoupling capacitor (C_E, used to short circuit the emitter resistor, R_E, and to connect the emitter in AC to the ground). The capacitors have a very low reactance at the working frequency (several ohms ÷ tens of ohms). The amplitude of the AC voltage (V_S) source is smaller than the thermal voltage (V_{th}). In AC, the input voltage (V_S) is applied between the base and the emitter, and the output voltage (the load voltage) is measured between the collector and the emitter. Thus, the emitter is common to both input and output. This is also the reason why the amplifier is called a "common emitter".
The DC schematic for the common emitter amplifier is represented in Fig.17. The voltage divider formed by R_{B1} and R_{B2} provides a constant base voltage (proportional to V_{CC} – which is supposed to be a regulated supply voltage). The current flowing through the voltage divider must be chosen at least 10 times higher than the base current of the transistor (the change of base current should have a very small effect on the modification of the base potential). The emitter resistor (R_E) introduces a DC negative feedback to keep almost constant the collector current, when the base potential and (or) the ambient temperature are changing. For a stable operation, the I_C must be kept constant, and biasing the BJT at constant V_{BE} (without the emitter resistor R_E) is a wrong decision (it has been previously shown that V_{BE}, V_{th} and I_S strongly dependent on temperature). R_E also reduces the output swing.

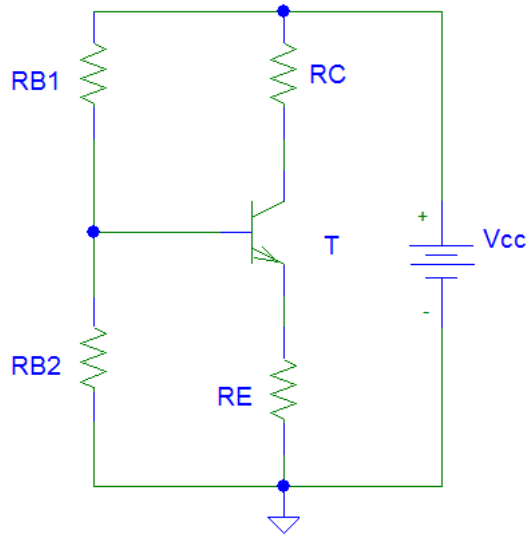


Fig.17.The DC circuit for the common emitter amplifier

It can be written as:

$$\frac{R_{B2}}{R_{B1}+R_{B2}}\cdot V_{CC}=\frac{R_{B1}\cdot R_{B2}}{R_{B1}+R_{B2}}\cdot\frac{I_C}{\beta_F}+V_{BE}+\frac{\beta_F+1}{\beta_F}\cdot R_E\cdot I_C \tag{32}$$

$$V_{CC}=R_C\cdot I_C+V_{CE}+\frac{\beta_F+1}{\beta_F}\cdot R_E\cdot I_C \tag{33}$$

It results:

$$I_C=\frac{\frac{R_{B2}}{R_{B1}+R_{B2}}\cdot V_{CC}-V_{BE}}{\frac{R_{B1}\cdot R_{B2}}{R_{B1}+R_{B2}}\cdot\frac{1}{\beta_F}+\frac{\beta_F+1}{\beta_F}\cdot R_E} \tag{34}$$

$$V_{CE} = V_{CC} - \left(R_C + \frac{\beta_F + 1}{\beta_F} \cdot R_E \right) \cdot I_C \tag{35}$$

$$V_{CE} = V_{CC} - \left(R_C + \frac{\beta_F + 1}{\beta_F} \cdot R_E \right) \cdot \frac{\frac{R_{B2}}{R_{B1} + R_{B2}} \cdot V_{CC} - V_{BE}}{\frac{R_{B1} \cdot R_{B2}}{R_{B1} + R_{B2}} \cdot \frac{1}{\beta_F} + \frac{\beta_F + 1}{\beta_F} \cdot R_E} \tag{36}$$

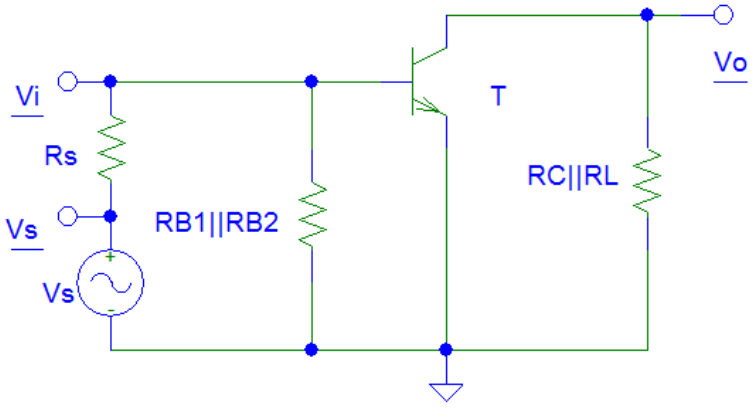
The transfer conductance is:

$$g_m = 40 \cdot I_C (mA/V) \tag{37}$$

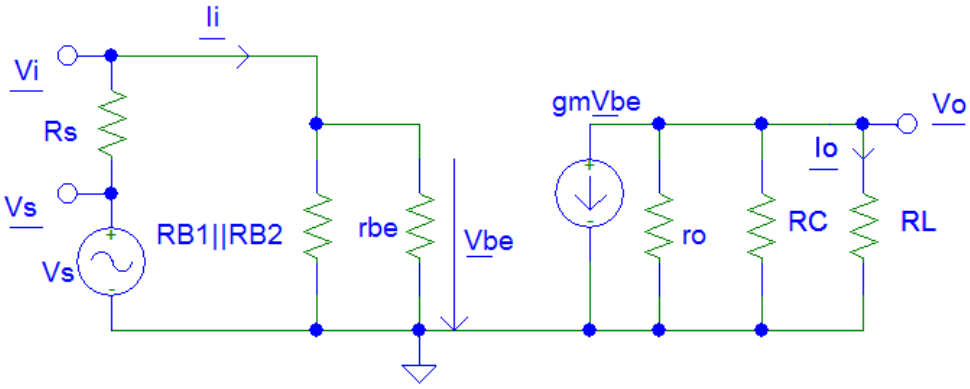
The input resistance of the BJT is:

$$r_{be} = \frac{\beta_0}{g_m} = \frac{h_{fe}}{g_m} \tag{38}$$

The AC schematic for the common emitter amplifier is represented in Fig.18.



a)



b)

Fig.18.The AC circuit for the common emitter amplifier:
a) by considering the BJT; b) by replacing the BJT with its small signal low frequency equivalent circuit

The voltage gain is:

$$\underline{A_V} = \frac{\underline{V_O}}{\underline{V_i}} = \frac{-g_m \cdot \underline{V_{be}} \cdot \left(r_O \parallel R_C \parallel R_L \right)}{\underline{V_{be}}} = -g_m \cdot \left(r_O \parallel R_C \parallel R_L \right) \tag{39}$$

The current gain of the circuit is:

$$\underline{A_I} = \frac{\underline{I_O}}{\underline{I_i}} = \frac{-g_m \cdot \underline{V_{be}} \cdot \dfrac{R_C \cdot r_O}{R_C \cdot r_O + R_L \cdot r_O + R_C \cdot R_L}}{\dfrac{\underline{V_{be}}}{\left(R_{B1} \parallel R_{B2} \parallel r_{be}\right)}} = -g_m \cdot \left(R_{B1} \parallel R_{B2} \parallel r_{be}\right) \cdot \frac{R_C \cdot r_O}{R_C \cdot r_O + R_L \cdot r_O + R_C \cdot R_L} \quad (40)$$

The transimpedance gain and the transconductance gain are:

$$\underline{A_Z} = \frac{\underline{V_O}}{\underline{I_i}} = \frac{-g_m \cdot \underline{V_{be}} \cdot \left(r_O \parallel R_C \parallel R_L\right)}{\dfrac{\underline{V_{be}}}{\left(R_{B1} \parallel R_{B2} \parallel r_{be}\right)}} = -g_m \cdot \left(r_O \parallel R_C \parallel R_L\right) \cdot \left(R_{B1} \parallel R_{B2} \parallel r_{be}\right) \quad (41)$$

$$\underline{A_Y} = \frac{\underline{I_O}}{\underline{V_i}} = \frac{-g_m \cdot \underline{V_{be}} \cdot \dfrac{R_C \cdot r_O}{R_C \cdot r_O + R_L \cdot r_O + R_C \cdot R_L}}{\underline{V_{be}}} = -g_m \cdot \frac{R_C \cdot r_O}{R_C \cdot r_O + R_L \cdot r_O + R_C \cdot R_L} \quad (42)$$

The output resistance (r_O) of the BJT is typically much higher compared to R_C and R_L, and the circuit can be simplified by eliminating it. Thus, the Eq. (39-42) can be simplified.

Linearity problems

Let's consider a simplified schematic of the common emitter amplifier (Fig.19):

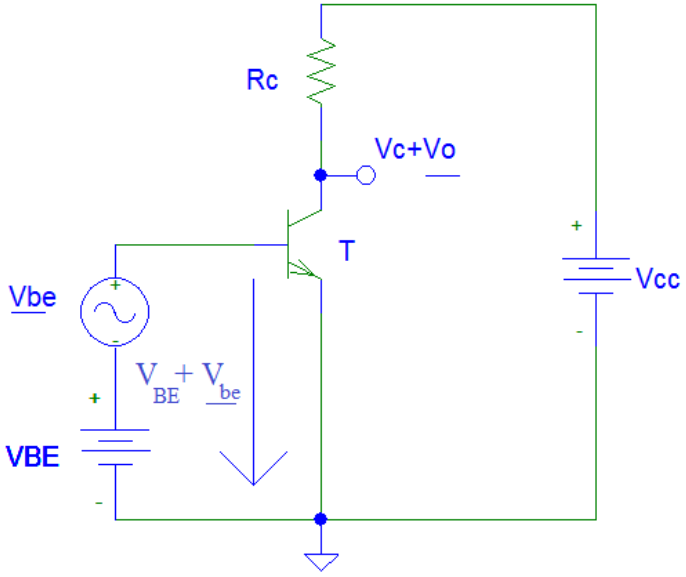


Fig.19. A simplified version of the common emitter amplifier

Looking at equation (3), it can be seen that the bipolar transistor has a strong nonlinear (exponential) transfer characteristic. The DC collector voltage is:

$$V_C = V_{CC} - R_C \cdot I_C \quad (43)$$

Considering equation (3) and neglecting the Early effect, equation (43) becomes:

$$V_C = V_{CC} - R_C \cdot I_C = V_{CC} - R_C \cdot I_S \cdot \exp\left(\frac{V_{BE}}{V_{th}}\right) \quad (44)$$

When an AC signal is applied to the input, the Eq.(44) can be developed in Taylor series:

$$V_C + \underline{V_O} = V_{CC} - R_C \cdot I_C \cdot \left(1 + \frac{\underline{V_{be}}}{V_{th}} + \frac{1}{2} \cdot \left(\frac{\underline{V_{be}}}{V_{th}} \right)^2 + ... \right) \tag{45}$$

In the situation when the input signal has a small amplitude, $|\underline{V_{be}}| \ll V_{th}$, so the quadratic and higher terms may be neglected. The equation becomes linear ($|\underline{V_{be}}| \ll V_{th}$):

$$V_C + \underline{V_O} = V_{CC} - R_C \cdot I_C \cdot \left(1 + \frac{\underline{V_{be}}}{V_{th}} \right) \tag{46}$$

The DC and the AC components are:

$$V_C = V_{CC} - R_C \cdot I_C \tag{47}$$

$$\underline{V_O} = -R_C \cdot I_C \cdot \frac{\underline{V_{be}}}{V_{th}} = -R_C \cdot \frac{I_C}{V_{th}} \cdot \underline{V_{be}} = -R_C \cdot g_m \cdot \underline{V_{be}} \tag{48}$$

By looking at Eq.(45), the ratio between the quadratic term to linear term is $\frac{\underline{V_{be}}}{2 \cdot V_{th}}$. If $\frac{|\underline{V_{be}}|}{2 \cdot V_{th}} = \frac{1}{5}$, a distortion of about twenty percent can be found in the output signal (this means that $|\underline{V_{be}}| = 10mV$). The conclusion is that the common emitter amplifier is linear only if the input signal has very low amplitudes. The operating point must be chosen so as to avoid saturation or transistor blocking, for the selected input voltage range (Fig.20).

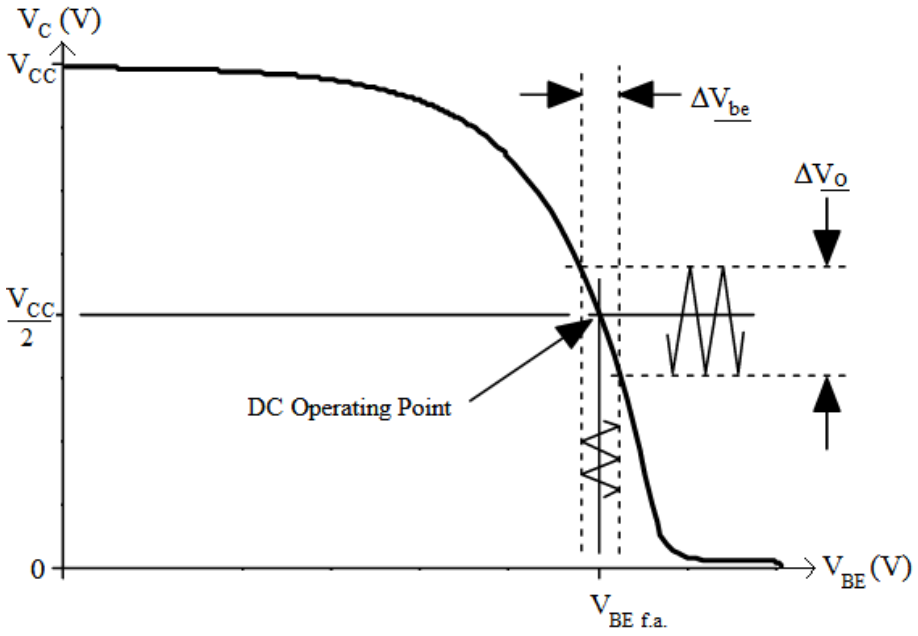


Fig.20. Choosing the DC operating point for the common emitter amplifier

7. Laboratory activity

a. BJT transfer characteristics

Consider the circuit given in Fig.21. The components are described in *Table 1* from Annex 1. It is required to draw and to simulate the circuit. VBE and VCC are DC voltage supplies.

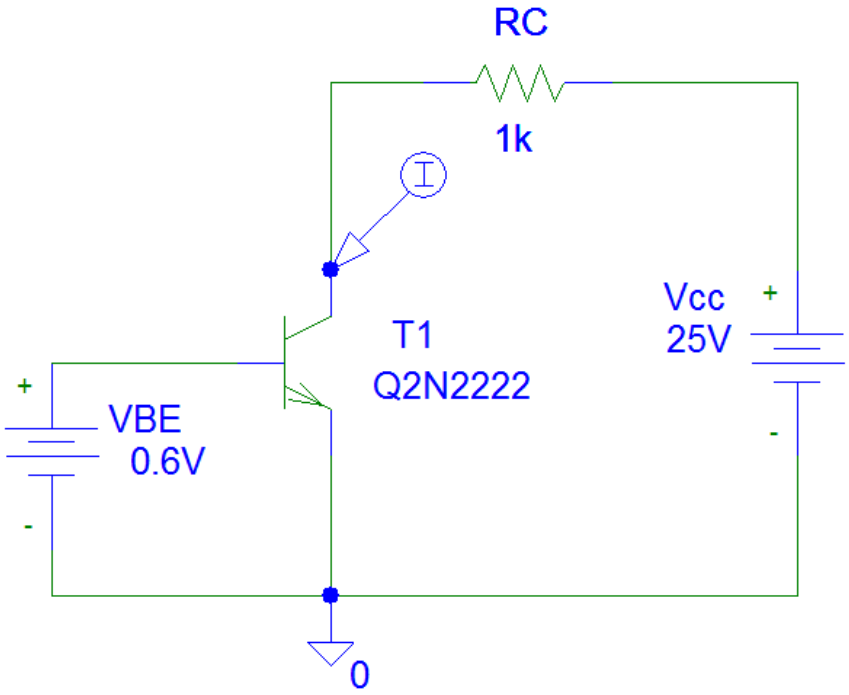


Fig.21 BJT schematic for measuring the transfer characteristics

The collector current (I_C) will be measured as a function of the base-emitter voltage (V_{BE}). To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is VBE. It will be varied between 0 and 0.7V with an increment of 0.01V (Fig.22).

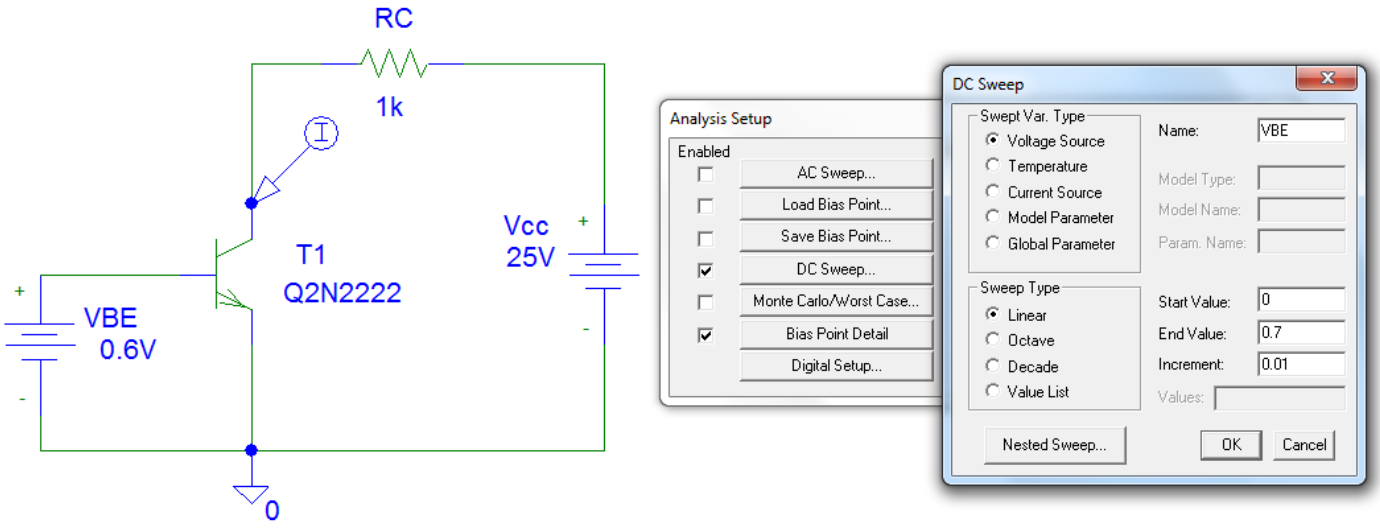


Fig.22 Adjusting VBE for measuring the transfer characteristics

The secondary DC sweep voltage (*Nested Sweep*….) is Vcc. It will be varied between 20V and 40V with an increment of 10V. The *Enable Nested Sweep* option will be checked (Fig.23).

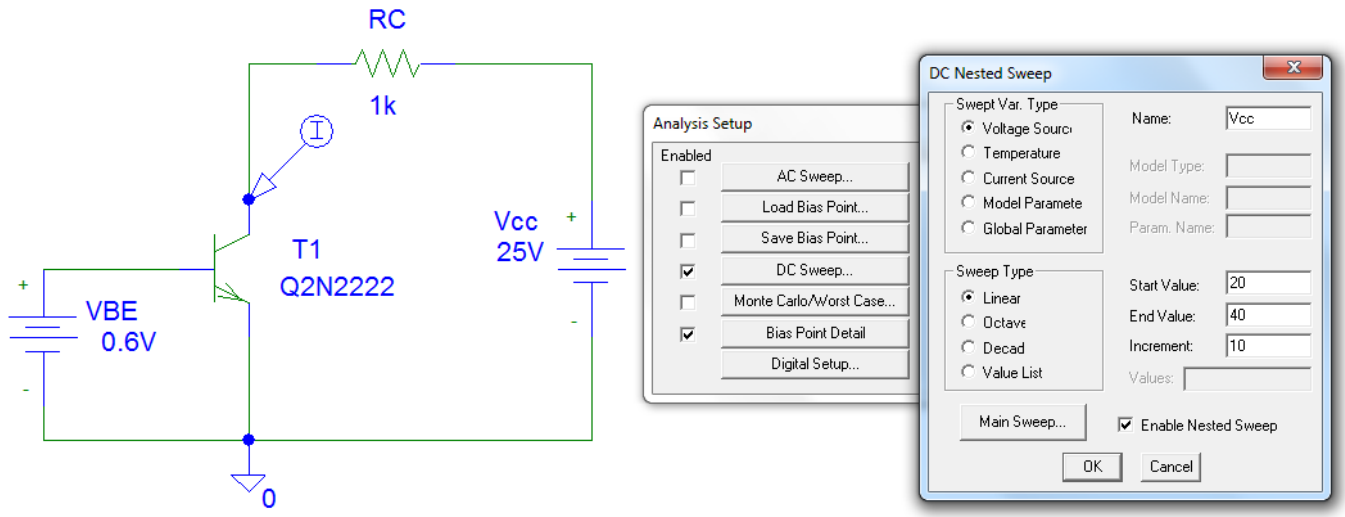


Fig.23 Adjusting Vcc for measuring the transfer characteristics

After running the simulation (F11), the collector current will be displayed on Y axis. For the X axis, the selected parameter will be the base-emitter voltage (V_{BE}) (Fig.24). By selecting the Toggle Cursor, the simulation results may be displayed.

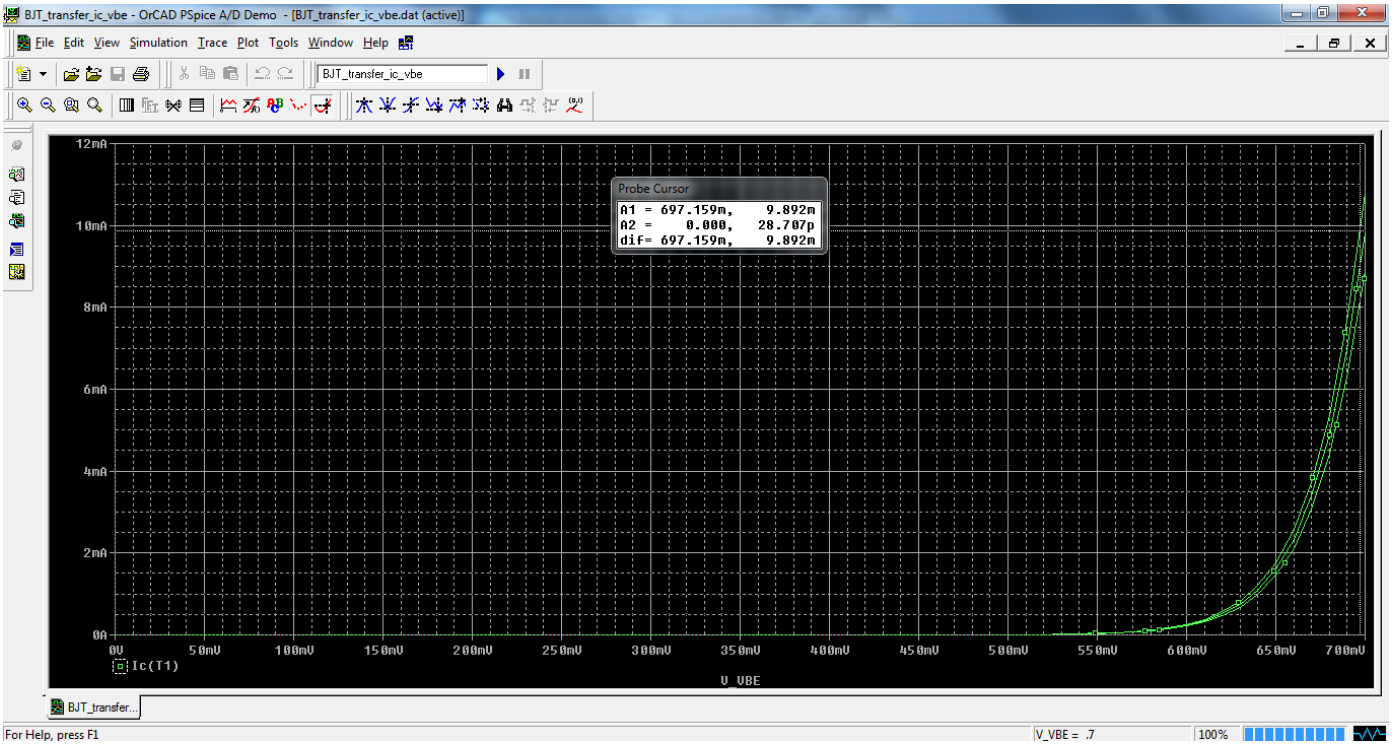


Fig.24 The measurement of the transfer characteristics I_C –V_{BE} for the npn BJT

The results should be written and complete Table 6.

Table 6 – BJT transfer characteristics

V_{CC}(V)	V_{BE}(mV)	I_C(mA)
20	0	
	500	
	550	
	600	
	650	
	700	
30	0	
	500	
	550	
	600	
	650	
	700	
40	0	
	500	
	550	
	600	
	650	
	700	

The effect of the Early voltage on the transfer characteristic may be observed by replacing the secondary DC Sweep voltage (V_{CC}) by the Early voltage parameter: select *Model Parameter*, *Model Type: NPN* , *Model Name: Q2N2222*, *Param. Name =VAF*, *Start Value: 20*, *End Value: 120*, *Increment: 50* (Fig.25).

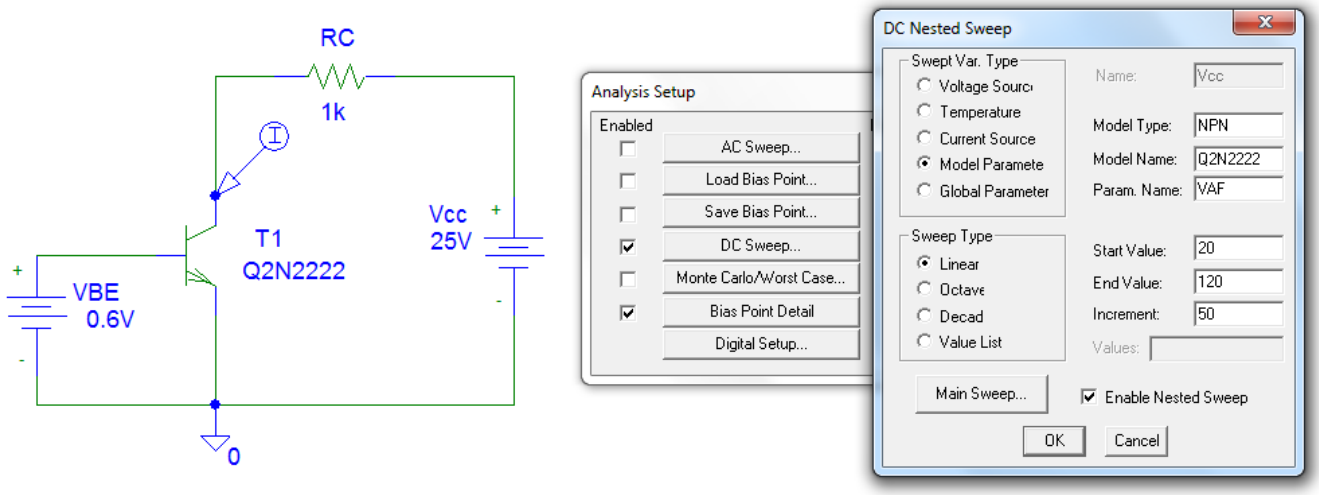


Fig.25 The Early voltage parameter settings to study its influence on the transfer characteristics

The simulation results (Fig.26) may be written in *Table 7*.

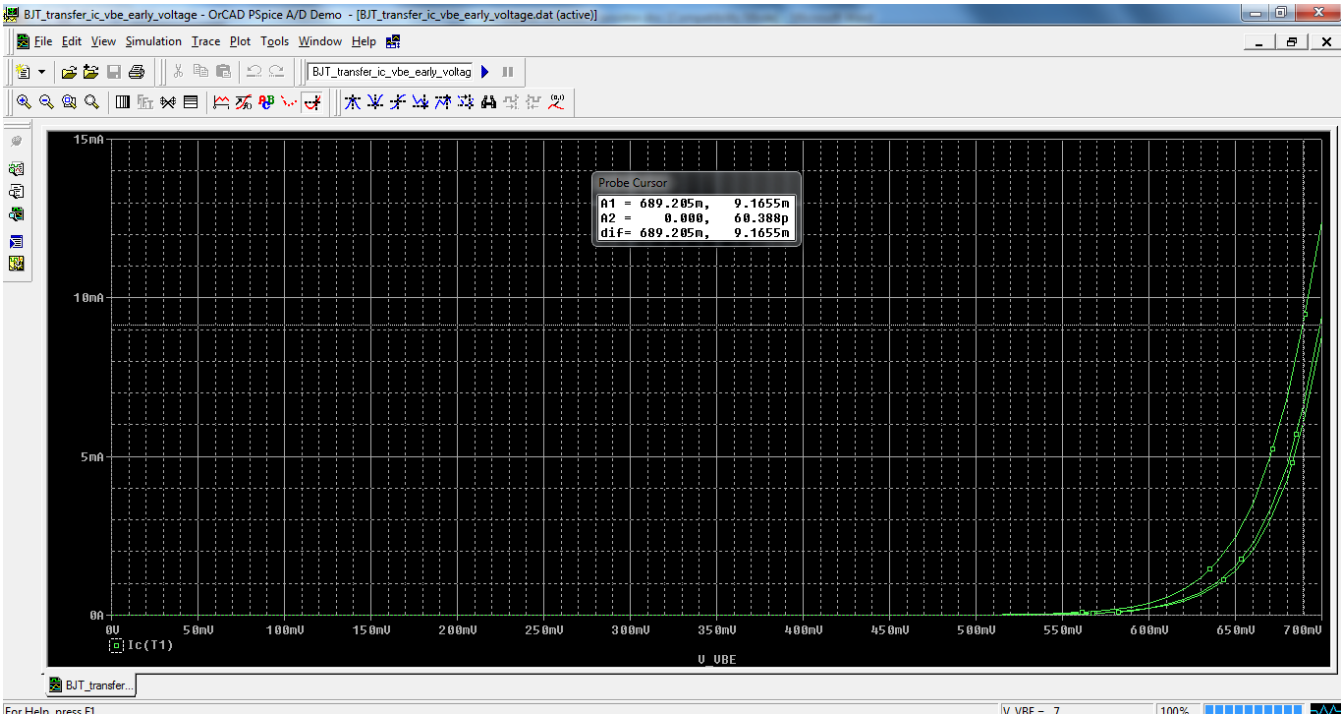


Fig.26 The influence of the Early voltage on the output current in the transfer characteristics

Table 7 – The influence of the Early voltage on the BJT transfer characteristics

V_A(V)	V_{BE}(mV)	I_C(mA)
20	0	
	500	
	550	
	600	
	650	
	700	
70	0	
	500	
	550	
	600	
	650	
	700	
120	0	
	500	
	550	
	600	
	650	
	700	

The temperature influence on the transfer characteristic may be studied if the temperature is set as the secondary DC Sweep parameter: *Nested Sweep...Temperature, Start Value: 20, End Value: 100, Increment: 40, Enable Nested Sweep* (Fig.27). To keep the transistor in the forward-active regime for the entire temperature range, R_C will be decreased to the value of 100Ω.

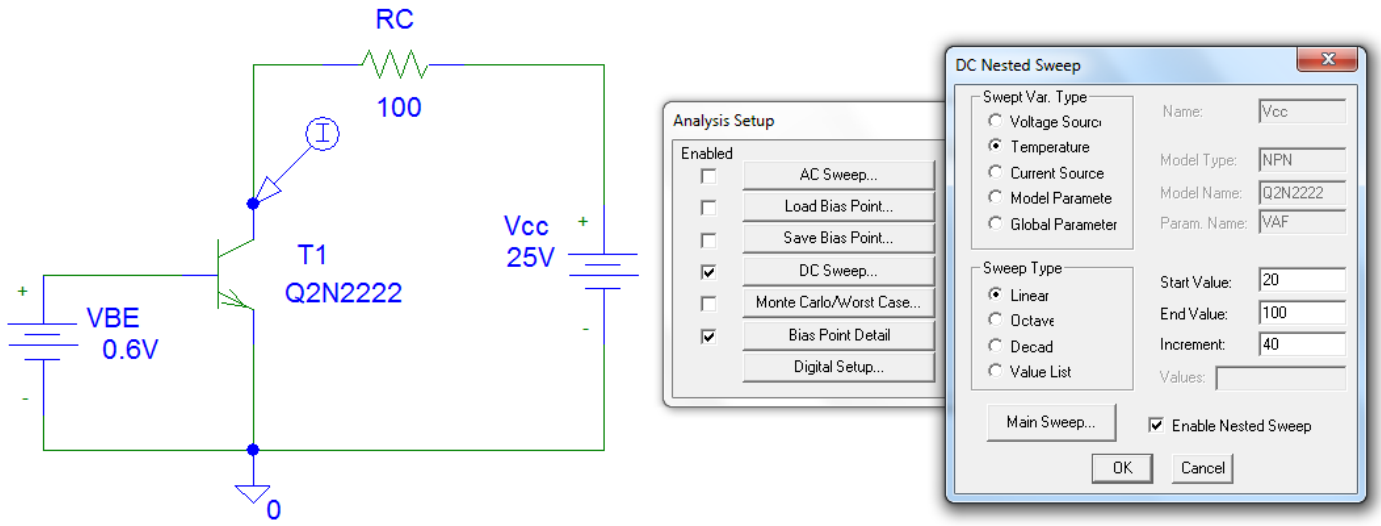


Fig.27.The temperature settings to study its influence on the transfer characteristics

The simulation results (Fig.28) will be depicted in Table 8.

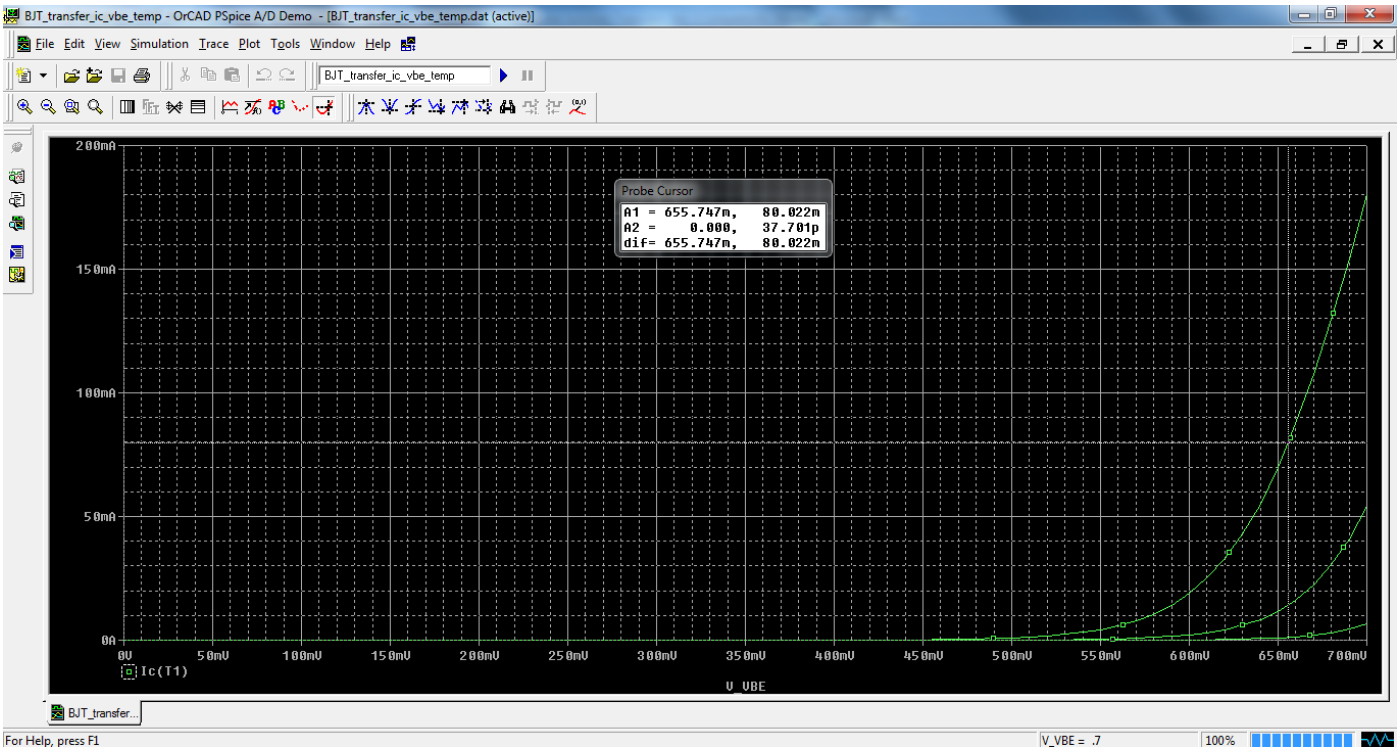


Fig.28.The temperature influence on the transfer characteristics

Table 8 – The influence of the temperature on the BJT transfer characteristics

t(^{0}C)	V_{BE}(mV)	I_C(mA)
20	0	
	500	
	550	
	600	
	650	
	700	
60	0	
	500	
	550	
	600	
	650	
	700	
100	0	
	500	
	550	
	600	
	650	
	700	

The $I_c = f(I_B)$ characteristic can be represented by drawing the circuit from Fig. 21 and by selecting the base current on the X axis: *Plot-Axis Settings...-X Axis - Axis Variable...- IB(T1).*

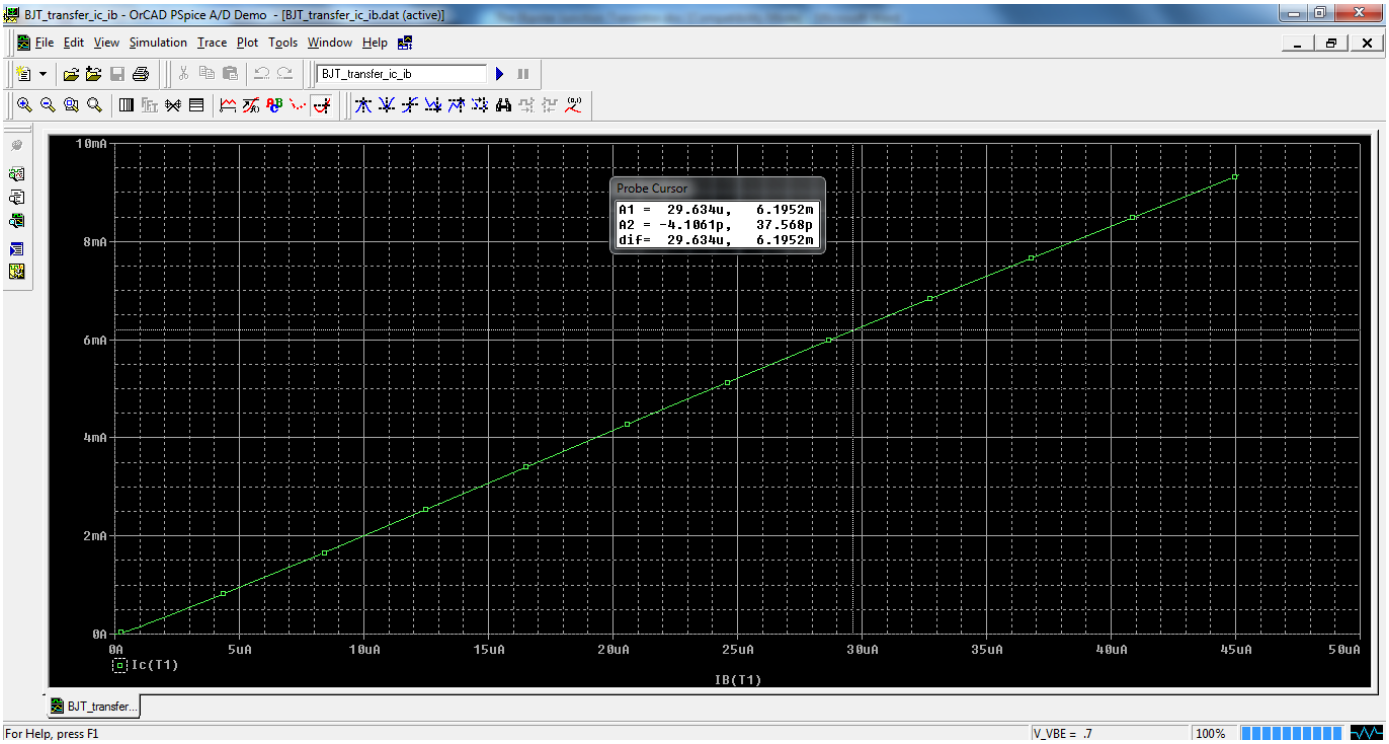


Fig.29.The Ic=f(I_B) transfer characteristic

The results may be collected in *Table 9*.

Table 9 – The Ic=f(I_B) transfer characteristic

I_B(µA)	I_C(mA)
0	
5	
10	
15	
20	
25	
30	
35	
40	
45	

The β_F dependence on I_C may be represented (Fig.30) if the collector current is set on the X axis (*Plot-Axis Settings...-X Axis - Axis Variable...- IC(T1)*) and β_F is displayed as a ratio between I_C and I_B (*Trace-Add Trace..- IC(T1)/IB(T1)*). The results are written in *Table 10*.

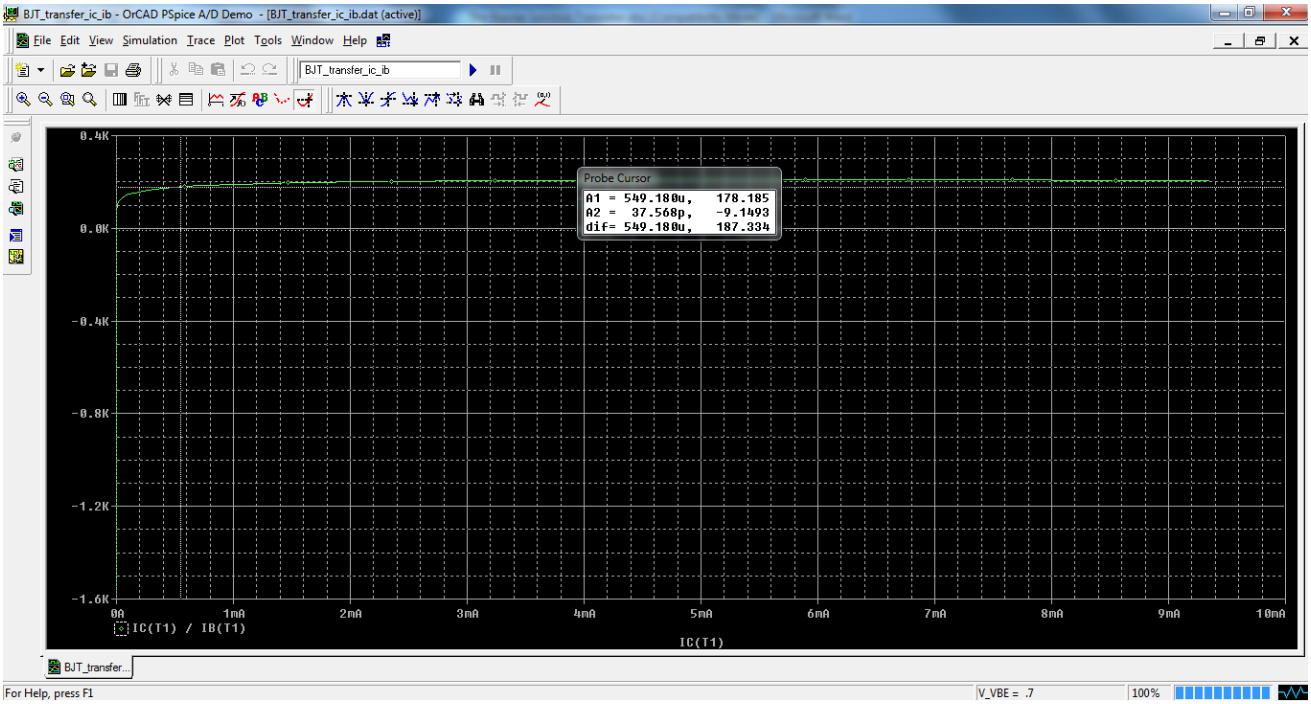


Fig.30. The β_F variation with Ic

Table 10 – The β_F change with Ic

I_c(mA)	β_F
0.005	
0.01	
0.05	
0.1	
0.2	
0.3	
0.5	
1	
5	
9	

b. BJT input characteristic

The BJT input characteristic $I_B=f(V_{BE})$ may be represented by using the circuit from Fig.21. The current marker should be connected in the base terminal (Fig.31).

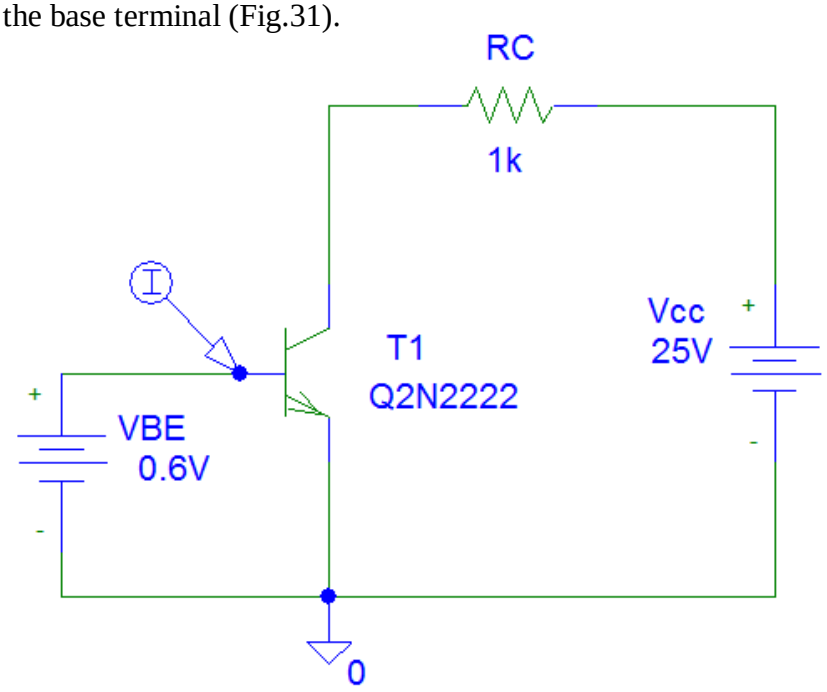


Fig.31. The setup for the input characteristic measurement ($I_B=f(V_{BE})$)

The simulation results (Fig.32) should be depicted in Table 11.

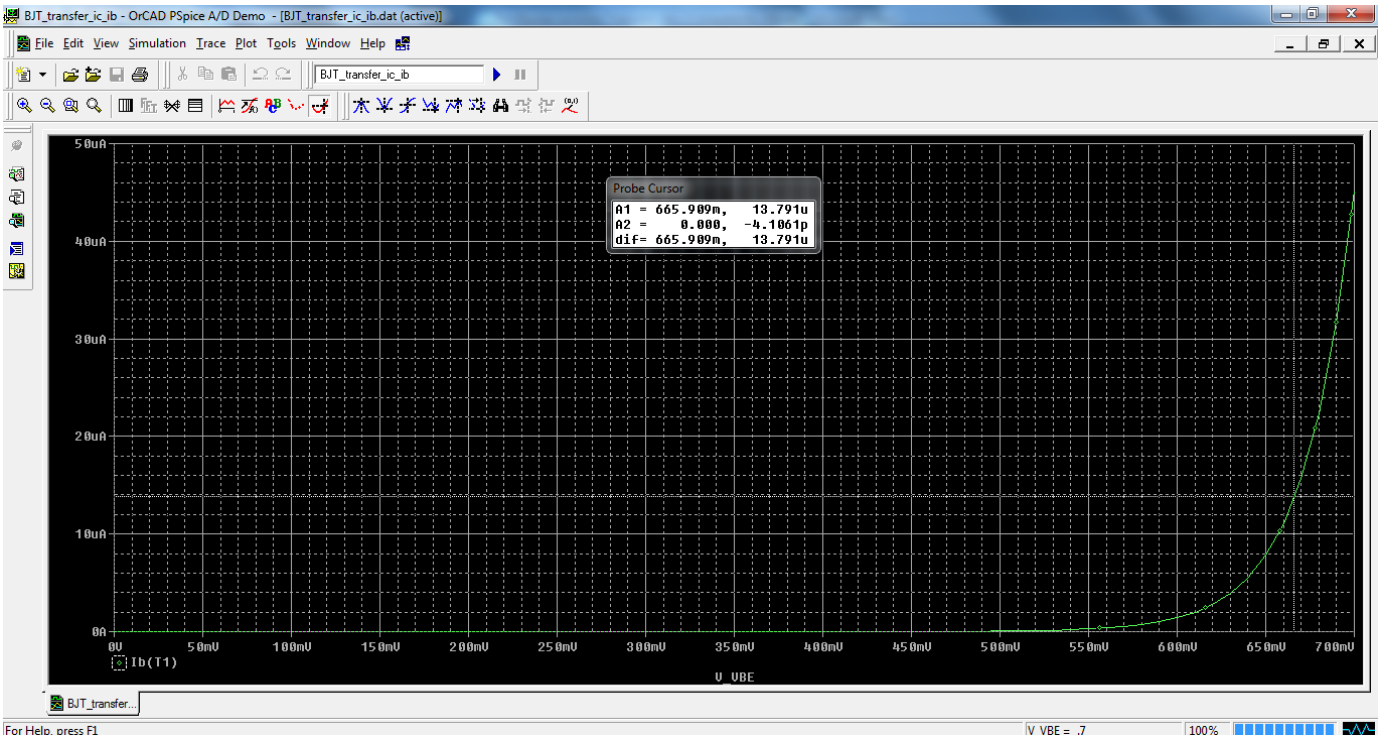


Fig.32. The input characteristic $I_B=f(V_{BE})$ for the npn BJT

Table 11 – The input characteristic Ic=f(V_{BE})

V_{BE}(mV)	I_B
0	
400	
500	
550	
600	
650	
700	

c. BJT output characteristic

Consider the circuit from Fig.21. The collector current (I_C) will be measured as a function of the collector-emitter voltage (V_{CE}) at different base-emitter discrete voltages. To do this task, a *DC Sweep…* analysis will be accomplished. The primary DC Sweep voltage is Vcc. It will be varied between 0 and 25V with an increment of 0.1V (Fig.33).

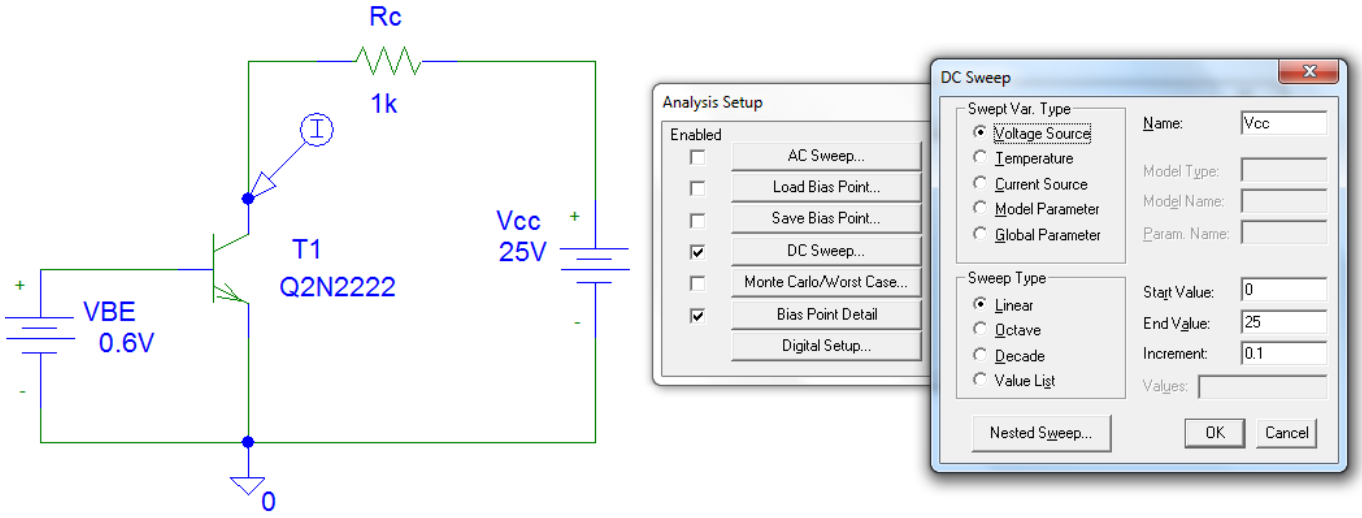


Fig.32. The setup for the supply voltage to measure the output characteristic I_C=f(V_{CE})

The second DC sweep voltage(*Nested Sweep….*) is the base-emitter voltage. It will be varied between 0.6 and 0.7V with an increment of 0.02V. The *Enable Nested Sweep* option will be checked (Fig.33).

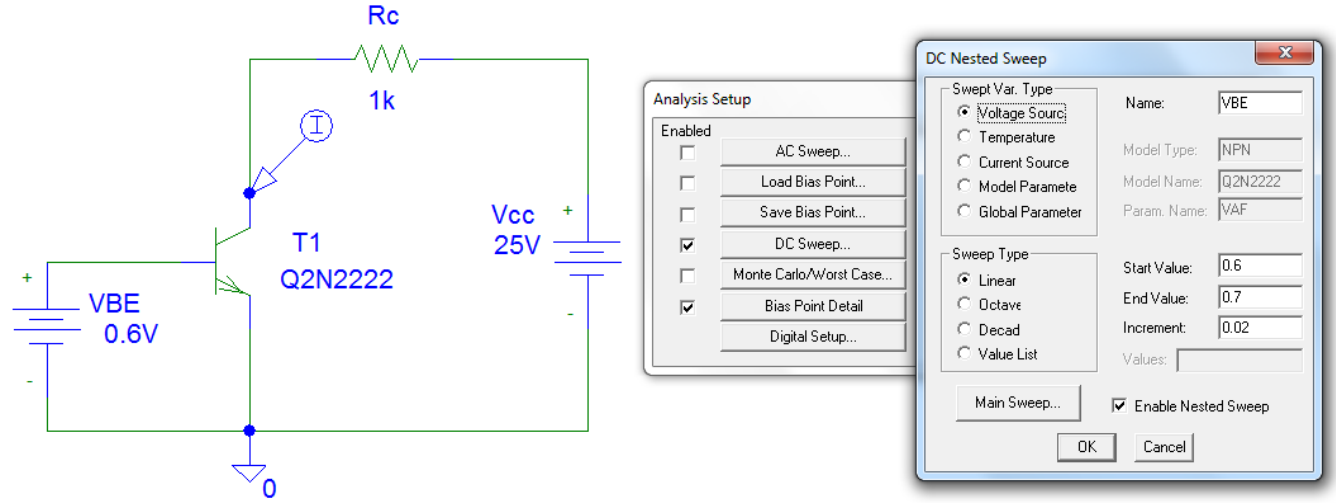


Fig.33. The setup for the base-emitter voltage to measure the output characteristic I_C=f(V_{CE})

Next step is to consider the display of the collector-emitter voltage (V_{CE}) in the *Orcad Pspice A/D Demo* probe window (*Plot-Axis Settings...-X Axis - Axis Variable...- VC(T1)*) (Fig.34). The inclination of the current-voltage characteristics is given by the Early voltage. The results should be noted in Table 12.

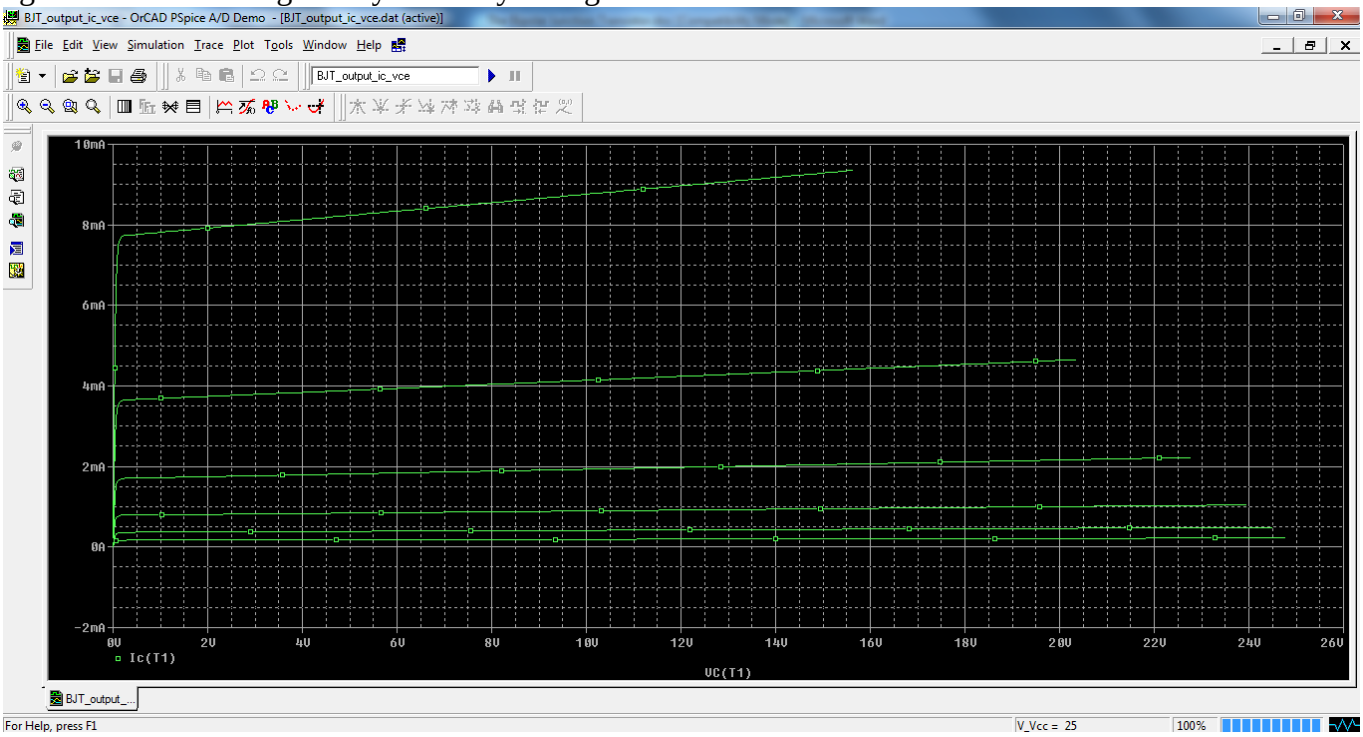


Fig.34. The output characteristic $I_C=f(V_{CE})$ for the npn BJT

Table 12 – BJT transfer characteristics

V_{BE}(mV)	V_{CE}(V)	I_C(mA)
600	0	
	0.01	
	0.05	
	0.1	
	0.2	
	0.5	
	1	
	2	
	4	
	8	
	16	
	24	
620	0	
	0.01	
	0.05	
	0.1	
	0.2	
	0.5	
	1	
	2	
	4	
	8	
	16	
	24	

640	0	
	0.05	
	0.1	
	0.2	
	0.5	
	1	
	2	
	4	
	8	
	16	
	22	
660	0	
	0.01	
	0.05	
	0.1	
	0.2	
	0.5	
	1	
	2	
	4	
	8	
	16	
680	0	
	0.01	
	0.05	
	0.1	
	0.2	
	0.5	
	1	
	2	
	4	
	8	
	16	
	24	
700	0	
	0.01	
	0.05	
	0.1	
	0.2	
	0.5	
	1	
	2	
	4	
	8	
	16	
	24	

d. The common emitter AC amplifier

Consider the small signal AC amplifier which uses a npn bipolar junction transistor in the common emitter configuration (Fig.35). The AC input signal (Vs) is provided by a sine-wave voltage source (VSIN), with the parameters: VOFF =0, VAMPL=1mV, FREQ=1k, TD=0, DF=0, PHASE=0. In the emitter is connected a 5KΩ potentiometer (RPOT, *VALUE =5k*) to adjust the DC collector current through the transistor (by changing the SET parameter taking the values from *Table 13*).

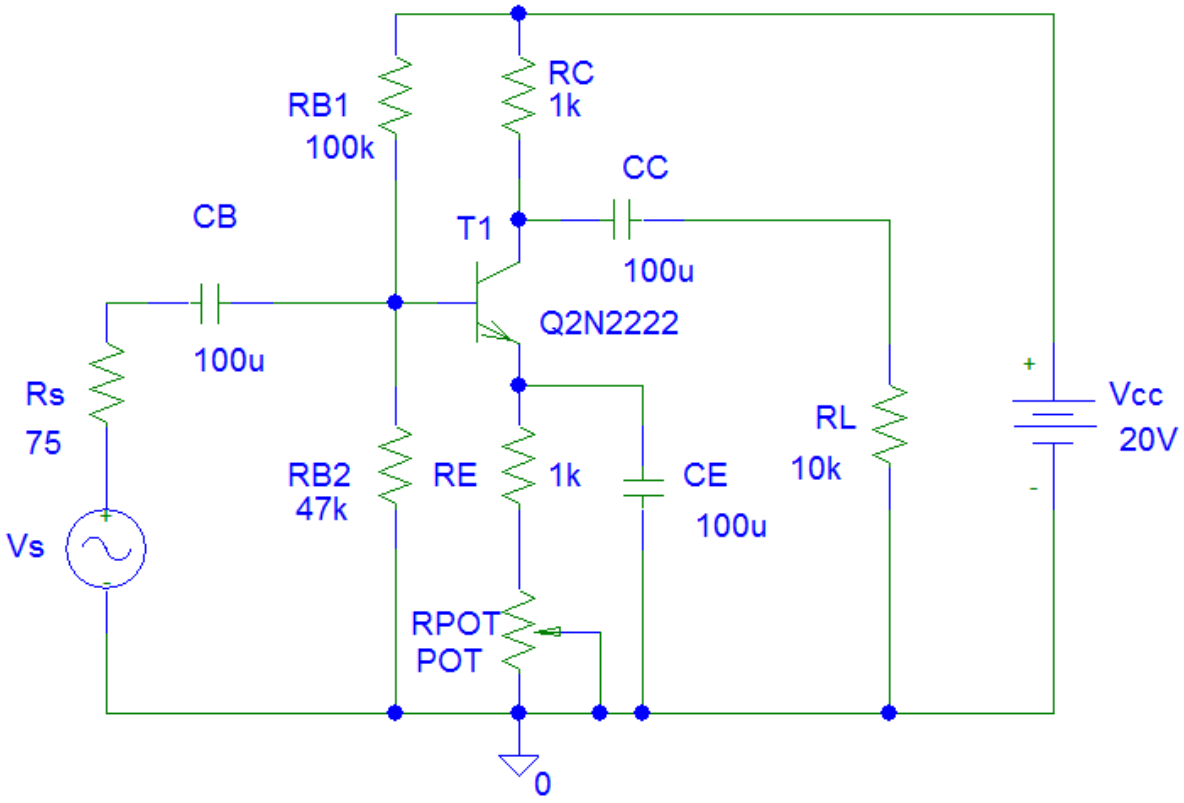


Fig.35.The common emitter amplifier with a npn BJT

The simulation should be performed in the time domain (*Transient*), for a time of about 10ms.

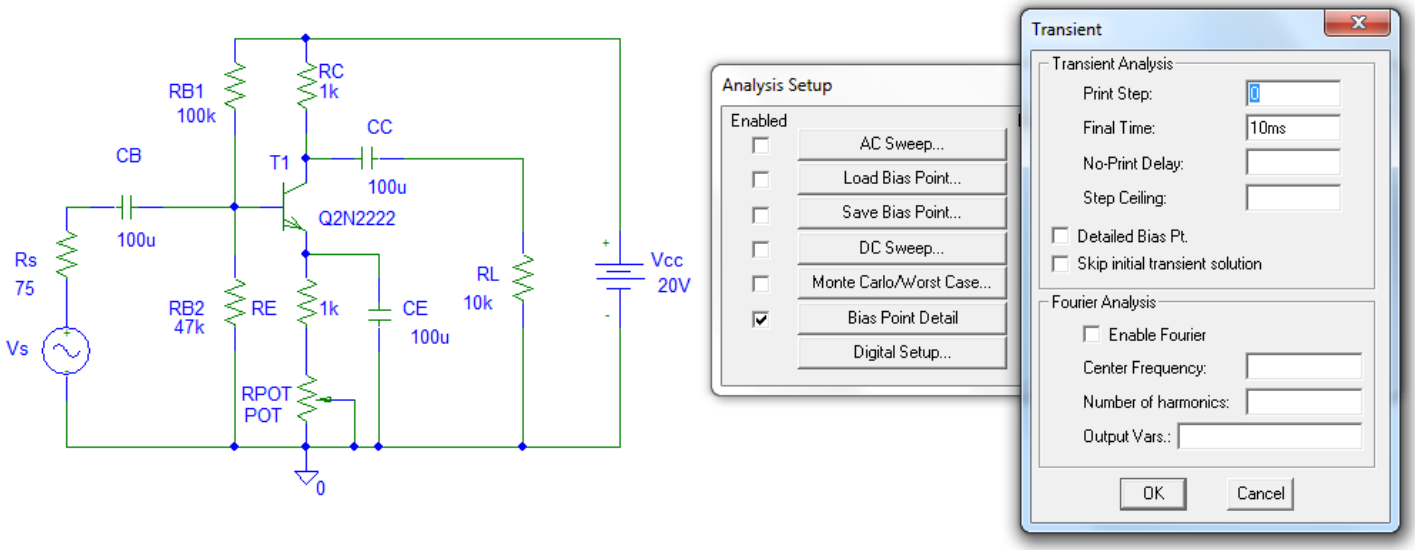


Fig.36. Selecting the Transient simulation for the small signal AC amplifier with BJT

The RMS values for the input (base) and output (collector) amplitudes may be monitored by selecting:

- *(MAX(V(T1:b)) - MIN(V(T1:b)))/(2*SQRT(2))* for the input voltage (V_b);
- *(MAX(V(T1:c)) - MIN(V(T1:c)))/(2*SQRT(2))* for the output voltage ($\underline{V_O}$);
- *(MAX(I(CB)) - MIN(I(CB)))/(2*SQRT(2))* for the input current ($\underline{I_i}$);
- *(MAX(I(RL)) - MIN(I(RL)))/(2*SQRT(2))* for the output current ($\underline{I_O}$).

The voltage AC gain is:

$$A_v = \frac{\underline{V_o}}{\underline{V_i}} = \frac{\text{(MAX(V(T1:c)) - MIN(V(T1:c)))/(2*SQRT(2))}}{\text{(MAX(V(T1:b)) - MIN(V(T1:b)))/(2*SQRT(2))}} \tag{49}$$

The current gain is:

$$A_i = \frac{\underline{I_o}}{\underline{I_i}} = \frac{\text{(MAX(I(RL)) - MIN(I(RL)))/(2*SQRT(2))}}{\text{(MAX(I(CB)) - MIN(I(CB)))/(2*SQRT(2))}} \tag{50}$$

The transimpedance gain is:

$$A_Z = \frac{\underline{V_o}}{\underline{I_i}} = \frac{\text{(MAX(V(T1:c)) - MIN(V(T1:c)))/(2*SQRT(2))}}{\text{(MAX(I(CB)) - MIN(I(CB)))/(2*SQRT(2))}} \tag{51}$$

The transadmitance gain is:

$$A_Y = \frac{\underline{I_o}}{\underline{V_i}} = \frac{\text{(MAX(I(RL)) - MIN(I(RL)))/(2*SQRT(2))}}{\text{(MAX(V(T1:b)) - MIN(V(T1:b)))/(2*SQRT(2))}} \tag{52}$$

The AC gains of the circuit should be depicted in *Table 13*.

Table 13 – The AC gain for the common emitter amplifier

SET	I_C(mA)	AC Gain
0.9		A_V=
		A_I=
		A_Z=
		A_Y=
0.33		A_V=
		A_I=
		A_Z=
		A_Y=
0.14		A_V=
		A_I=
		A_Z=
		A_Y=
0.05		A_V=
		A_I=
		A_Z=
		A_Y=
0		A_V=
		A_I=
		A_Z=
		A_Y=

An example which shows the simulation result for the voltage gain of the circuit is in Fig. 37.

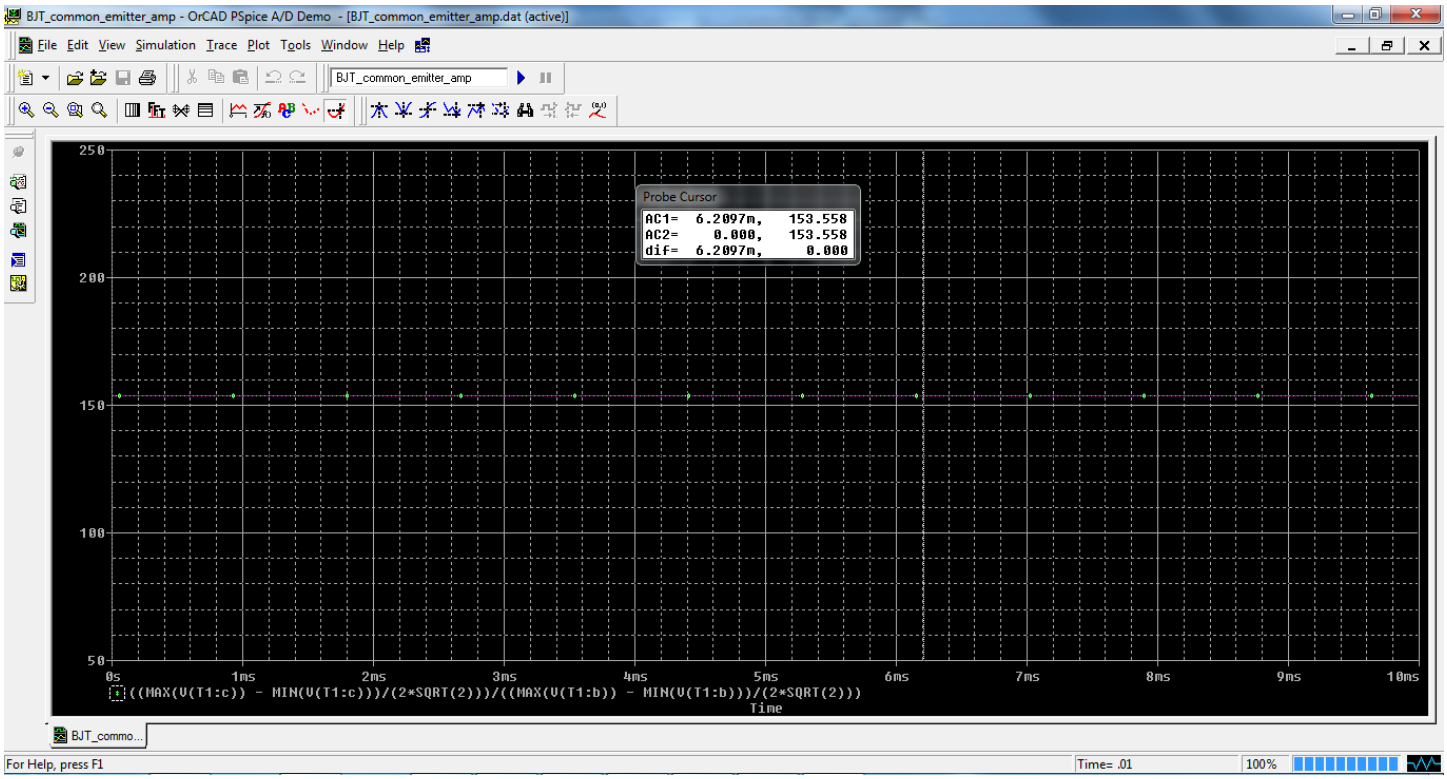


Fig.37. Measuring the voltage gain for the common emitter amplifier

Exercises

1. Compare the AC gains for the common emitter amplifier (with BJT) and the common source amplifiers (with JFET and MOSFET).
2. Measure and compare the input impedance for the the common emitter amplifier and the common source amplifiers.
3. What is the phase shift between the output and the input signals for the BJT amplifiers?
4. Compare the AC gains for common emitter amplifier at several DC collector currents.

Annex 1

Table 1

Pos.	Component type	Value	Library
1.	R (resistor)	Numerical value is taken from the laboratory platform. - Mili-ohms if *m* is written after the numerical value - Ohms if nothing is written after the numerical value - Kilo-ohms if *k* is written immediately after the numerical value - Mega-ohms if *meg* is written immediately after the numerical value	Analog.slb
2.	C (capacitor)	Numerical value is taken from the laboratory platform. - Pico-farads if *p* is written after the numerical value - nano-farads if *n* is written after the numerical value - micro-farads if *u* is written after the numerical value - mili-farads if *m* is written after the numerical value - farads if nothing is written after the numerical value	Analog.slb
2.	T1	Q2N2222 (npn-BJT)	Eval.slb
3.	POT	VALUE =5k ; SET is between 0 and 1 (the cursor position)	Breakout.slb
4.	VSIN (used to function as a signal generator, sine-wave voltage source for time domain analysis)	- **DC**: the DC component of the sine wave - **AC**: the AC value of the sine wave. - **VOFF**: the DC offset value (set to zero if you need a pure sinusoid). - **VAMPL**: the undamped amplitude of the sinusoid; i.e., the peak value measured from zero if there were no DC offset value. - **FREQ**: the frequency in Hz of the sinusoid. - **TD**: the time delay in seconds (set to zero for the normal sinusoid). - **DF**: damping factor (set to zero for the normal sinusoid). - **PHASE**: phase advance in degrees (set to 90 if you need a cosine wave form). Note: the normal usage of this source type is to set **VOFF**, **TD** and **DF** to zero as this will give you a 'nice' sine wave.	Source.slb
5.	VDC (simple DC voltage source)	- Value in volts.	Source.slb
6.	GND_ANALOG	- Ground (node potential is 0 volts). - It is **mandatory** to be used in any PSpice schematic!	Port.slb

Bibliography

1. Cadence Design Systems, PSpice User's guide, Second Edition, 31 May 2000, Portland, Oregon, USA
2. https://www.computerhistory.org/siliconengine/invention-of-the-point-contact-transistor/
3. http://www.ee.ic.ac.uk/pcheung/teaching/aero2_signals&systems/transistor%20circuit%20notes.pdf
4. http://web.mit.edu/klund/www/Dphysics.pdf
5. http://aries.ucsd.edu/NAJMABADI/CLASS/ECE65/06-W/NOTES/BJT1.pdf
6. https://inst.eecs.berkeley.edu/~ee105/fa14/lectures/Lecture10-BJT%20Physics.pdf